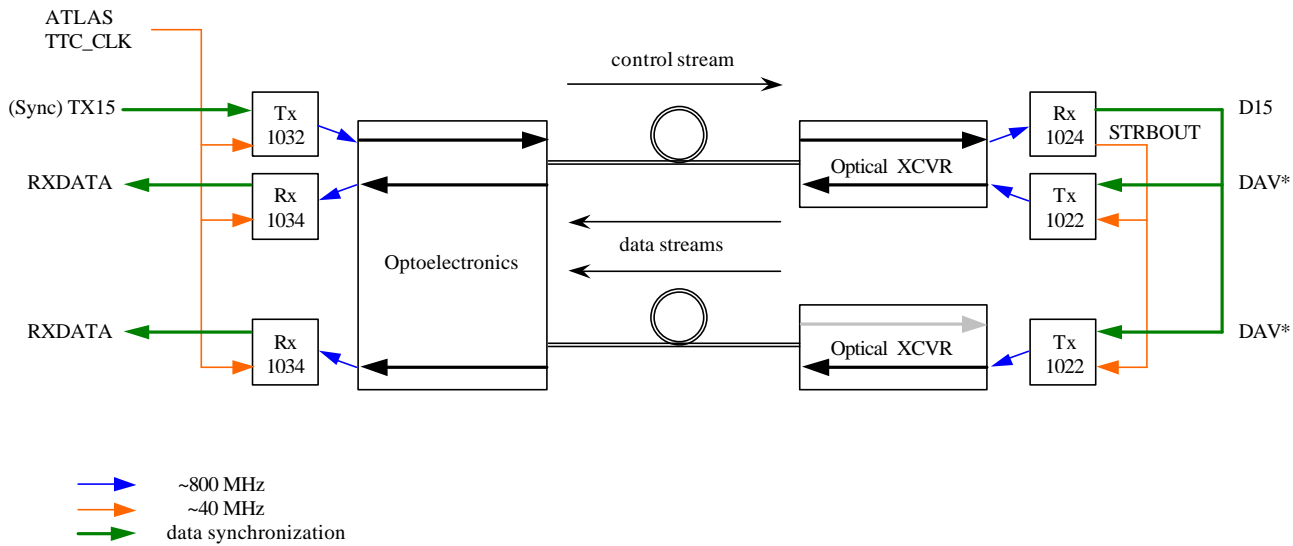


# CSC Transition Module / ASM II Link Maintenance



	Tx 1032	Rx 1024	Tx 1022	Rx 1034
board	TM	ASM II	ASM II	TM
stream information	clock, Sync, SCA control, etc.	clock, Sync, SCA control, etc.	ADC data	ADC data
word width	16 or 17 bits	16 or 17 bits	16 bits	16 bits
DAV* (1022/1024) TXDATA (1032) RXDATA (1034)	deactivated only to generate fill frames	always active except when lock is lost	connected to data bit of 1024	used by TM to identify incoming data
lock frequency on:	TTC_CLK	control stream fill frames	STRBOUT	TTC_CLK
lock phase on:	TTC_CLK	control stream frames	STRBOUT	data stream frames
loss of lock causes	power-up	SEU	SEU, bad STRBOUT (?)	bad data stream, laser disabled
how does the TM know that lock was lost?	1032 LOCKED signal	both 1034's lose lock	associated 1034 loses lock	1034 RXREADY signal
what does TM do when lock is lost?	wait	send fill frames	wait (unless both 1022's lose lock)	wait (unless both 1034's lose lock)
when are associated lasers disabled?	when 1034's lose lock for an extended period	N/A	when 1024 is not ready	N/A

The data synchronization mechanism helps the TM identify incoming ADC data. The TM's Sync signal is carried to the ASM II as one of the 1032's data bits, e.g., TX15. The ASM II routes the signal, which it sees as D15 on its 1024, to the DAV\* pins of its 1022's. The signal then appears to the TM as RXDATA (analogous to DAV\*) on its 1034's. The TM typically asserts Sync such that RXDATA is active only when incoming ADC data arrive at the TM. In addition to helping assess data integrity, the synchronization mechanism may help the TM maintain the link.

Nomenclature note: "control stream" refers to information sent by the TM to the ASM II, such as clock and SCA control. It does not refer to G-Link control frames. We only use G-Link data frames.

Tx 1032 Signals

Signal	I/O	Description	Connected to	Connection basis
TXCLK	I	word clock (40 MHz)	clock buffer	one point-to-point clock per-Tx
TXDIV0 TXDIV1	I	VCO divider select – these determine the operating frequency range of the VCO	TBD	TBD
TX[15:0]	I	40 MHz stream that controls the ASM II. Bits are used for Sync, SCA control, etc.	TX FPGA	per-chamber bus*
TXFLAG	I	this may be used as a 17 <sup>th</sup> data bit, use is TBD	TX FPGA	per-chamber bus*
TXDATA	I	when active, data frames are transmitted; when inactive, fill frames are transmitted	TX FPGA	per-Tx
TXCNTL	I	tied inactive – we do not use control frames	TX FPGA (optional)	per-Tx
LOCKED	O	active when PLL locks to TXCLK	TX FPGA (optional)	per-Tx
TXFLGENB	I	enables use of TXFLAG, use is TBD	TX FPGA	per-chamber bus*
ESMPXENB	I	tied inactive – we do not use enhanced simplex mode	TX FPGA (optional)	per-Tx
HSOUT+ HSOUT-	O	high-speed serial output	optical transmitter	per-Tx
TXCAP0 TXCAP1	-	loop filter capacitor	loop filter capacitor	per-Tx
TCLKENB	I	tied inactive – we do not use test clock mode	TX FPGA (optional)	per-Tx

For testing purposes, TCLKENB and/or ESMPXENB might be used to reset the ASM II's 1024 by sending codes that the 1024 does not recognize. I.e., SEU-induced loss of lock might be simulated.

“Optional” indicates that the signal is connected to an FPGA only if FPGA pins are available.

\* assumes per-chamber clock phase vernier

Rx 1034 Signals

Signal	I/O	Description	Connected to	Connection basis
REFCLK	I	word clock (40 MHz)	clock buffer	one point-to-point clock per-Rx
RXCLK0	O	recovered word rate clock – most outputs are updated on the rising edge of this clock when PASSENB is false – probably not used	RX FPGA (optional)	per-Rx
RXCLK1	O	inverse of RXCLK0 – not used	NC	
RXDIV0 RXDIV1	I	VCO divider select – these determine the operating frequency range of the VCO	TBD	TBD
RX[15:0]	O	40 MHz ADC data stream	RX FPGA	per-Rx
RXFLAG	O	this may be used as a 17 <sup>th</sup> data bit – not used	RX FPGA (optional)	per-Rx
RXDATA	O	when active, RX[15:0] contain valid data	RX FPGA	per-Rx
RXCNTL	O	not used – we do not use control frames	RX FPGA (optional)	per-Rx
RXREADY	O	indicates link is operating correctly	RX FPGA	per-Rx
RXERROR	O	per-word indication of an encoding error	RX FPGA	per-Rx
RXFLGENB	I	tied inactive – we do not use RXFLAG	RX FPGA (optional)	per-Rx
ESMPXENB	I	tied inactive – we do not use enhanced simplex mode	RX FPGA (optional)	per-chamber bus (?)
HSIN+ HSIN-	I	high-speed serial input	optical receiver	per-Rx
RXCAP0 RXCAP1	-	loop filter capacitor	loop filter capacitor	per-Rx
TSTCLK	I	tied high – we do not use test clock mode	tied high	-
#RESET	I	tied high – for test purposes only	tied high	-
WSYNCDDB	I	tied low – for test purposes only	tied low	-
PASSENB	I	tied inactive – we do not use the parallel automatic synchronization	RX FPGA (optional)	per-chamber bus (?)
RXDSLIP	O	these are used with the parallel automatic synchronization system	RX FPGA (optional)	per-Rx
SHFIN	I		SHFOUT	per-Rx
SHFOUT	O		SHFIN	per-Rx
SRQIN	I		tied low	-
SRQOUT	O		NC	-

“Optional” indicates that the signal is connected to an FPGA only if FPGA pins are available.