

ATLAS Cathode Strip Chambers  
Off-Detector Electronics

CSC ROD  
Hardware Final Design Review  
Production Readiness Review

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## **Slides to be Presented at Review**

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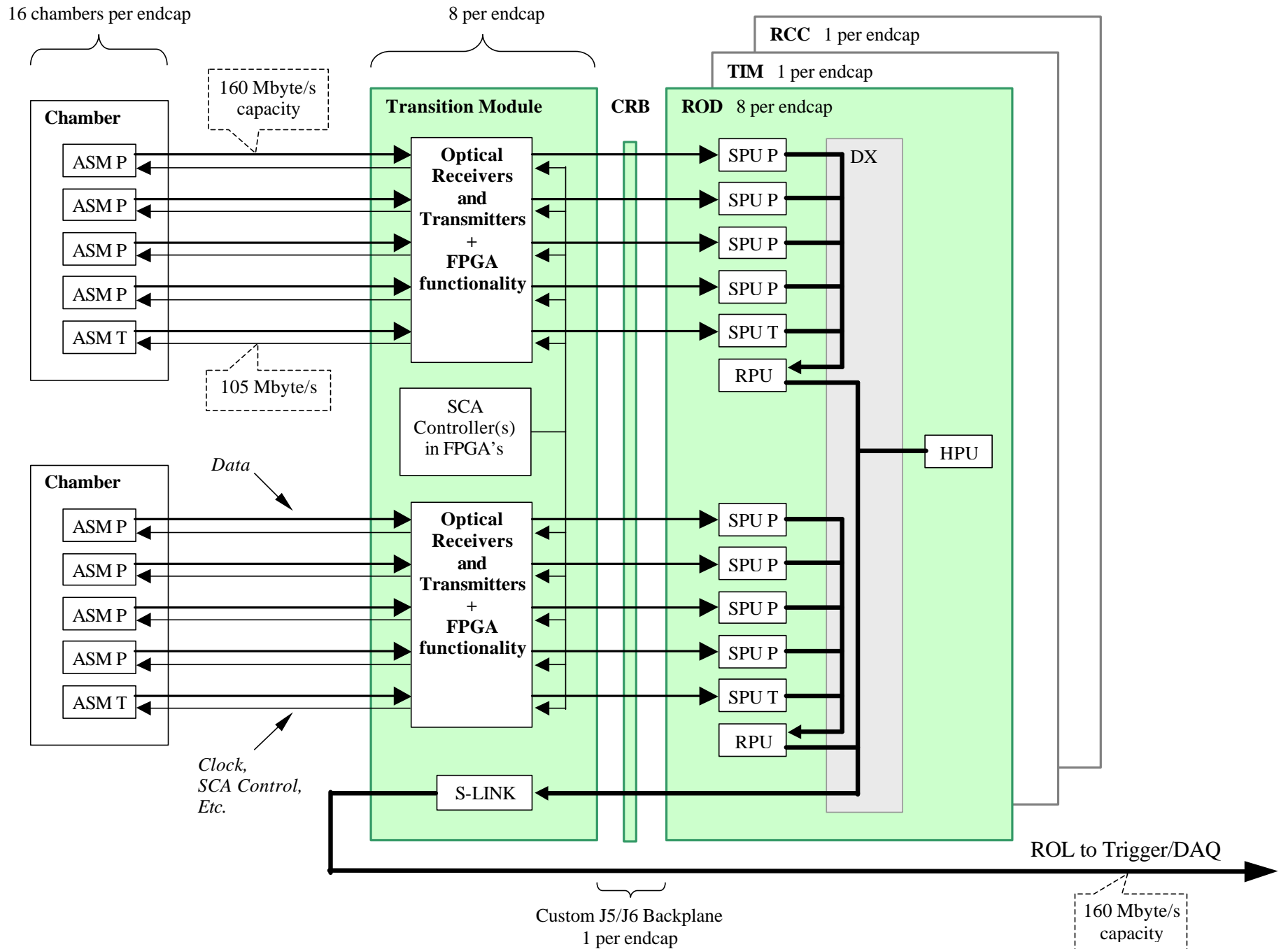
## **Supporting Slides**

- Nomenclature
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## Scope of Review

Item	Recommendation: In Scope?	Comment
<b>ROD Motherboard</b>		
detailed hardware functionality	no	Detailed hardware functionality is expressed in ~1 Mbyte of Verilog code. Coding and testing progress will be presented. For hardware design files, see Reference 1.
data path bandwidths	yes	
clock generation and distribution	yes	
signal integrity	yes	
power	yes	
testing	yes	
manufacturability	optional	The assembly house has studied the board and raised no concerns. A short run will be conducted before the final run. Most minor assembly defects can be readily reworked, but: BGA connectors are difficult to rework, and press-fit connectors (P0/P5/P6) are extremely difficult to rework. Given the extensive exercising of the ROD motherboard, it would be unwise to change the PCB unless absolutely necessary.
production plans	yes	
<b>GPU</b>		
design issues	no	The module has been extensively tested and exercised. Schematics are not available electronically.
testing	yes	
production plans	yes	
<b>CTM</b>	no	The CTM is subject to a separate review.
<b>Support Electronics</b>	no	Support Electronics are subject to a separate review.
<b>ROD Software</b>		
functionality	no	Software functionality is subject to a separate review.
performance	no	Software performance is subject to a separate review and has been demonstrated by prototype software.

# CSC Readout Electronics Overview



# Functional Summary: CSC Off-Detector Electronics

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## 1. Readout Drivers + CTM's

- Generate all control signals needed on-chamber, including SCA control.
- Transmit control signals and bunch crossing clock to chambers via optical G-Link.
- Accept digitized chamber data sent via optical G-Link (6.4 Gbit/s per chamber max).
- Check, sparsify (threshold and 75 ns window cuts), and reformat chamber data (SPU).
- Apply calibration constants (SPU and/or RPU).
- Reject neutrons and/or perform final out-of-time rejection (RPU).
- Orchestrate event building: SPU→RPU and RPU→output.
- Transmit events to Trigger/DAQ via S-LINK ROL.
- Monitor data, e.g., count errors, maintain statistics, fill histograms, etc. (SPU, RPU, HPU).
- Perform non-runtime functions such as system initialization and calibration runs (HPU).
- 9U boards, 16 ROD + 16 CTM boards service 32 chambers.

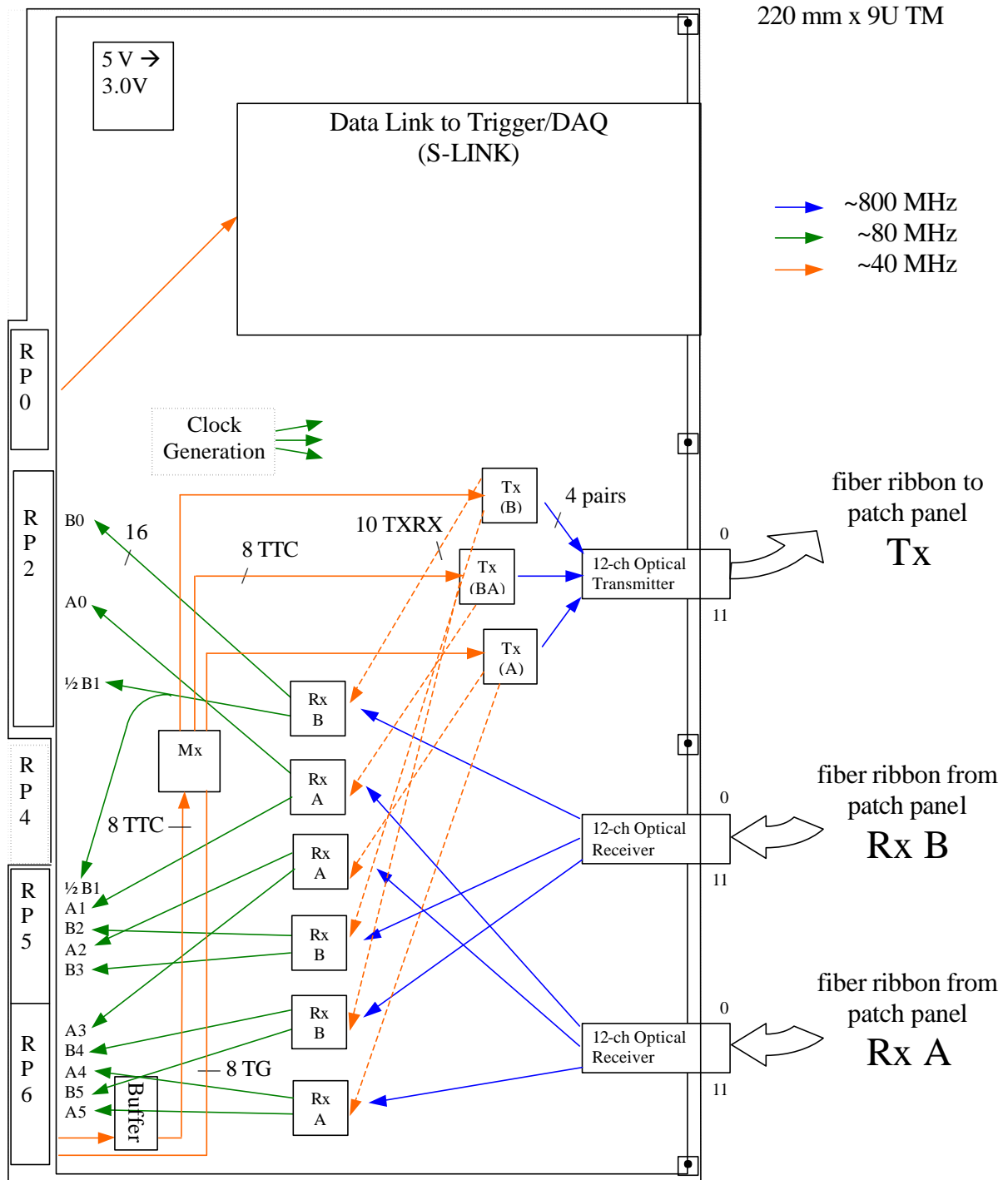
## 2. Support Electronics

- Physically support and supply power to ROD's, CTM's, TIM's, and RCC's.
- Interface CSC system to LHC and L1 timing via Timing Interface Module (TIM).
- Interface CSC system to ATLAS Trigger/DAQ, DCS, etc. via Ethernet.
- 1 9U VME crate per endcap with custom J5/J6 backplane.
- Each crate contains one RCC, one TIM, and 8 ROD's.
- Chamber count can be doubled with no additional support electronics.

## 3. Software

- DPU software + SPU algorithm runs in SPU DSP's on ROD's.
- DPU software + RPU algorithm runs in RPU DSP's on ROD's.
- HPU software runs in HPU DSP's on ROD's.
- RCC software runs in Rod Crate Controller.

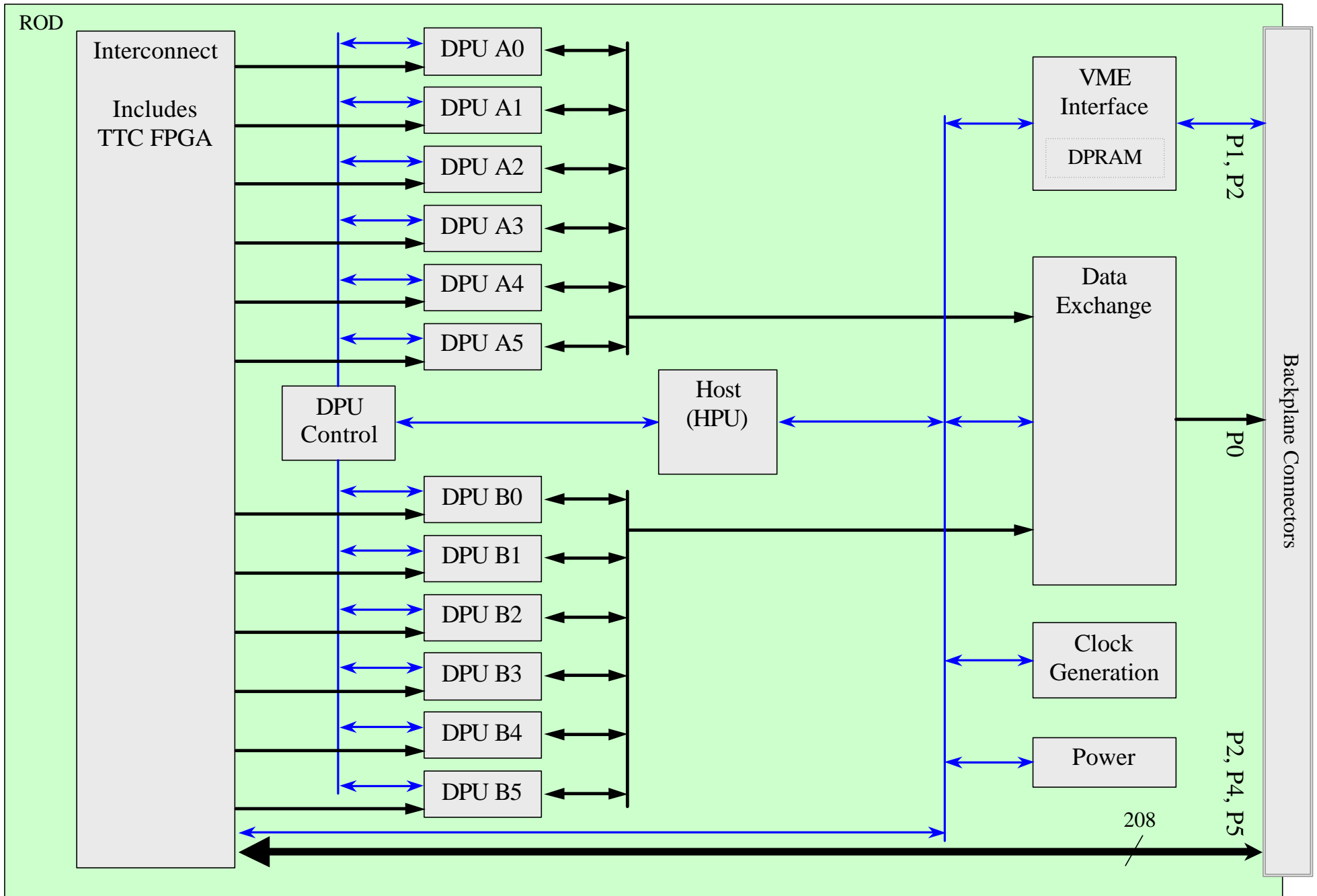
# CSC Transition Module (CTM)



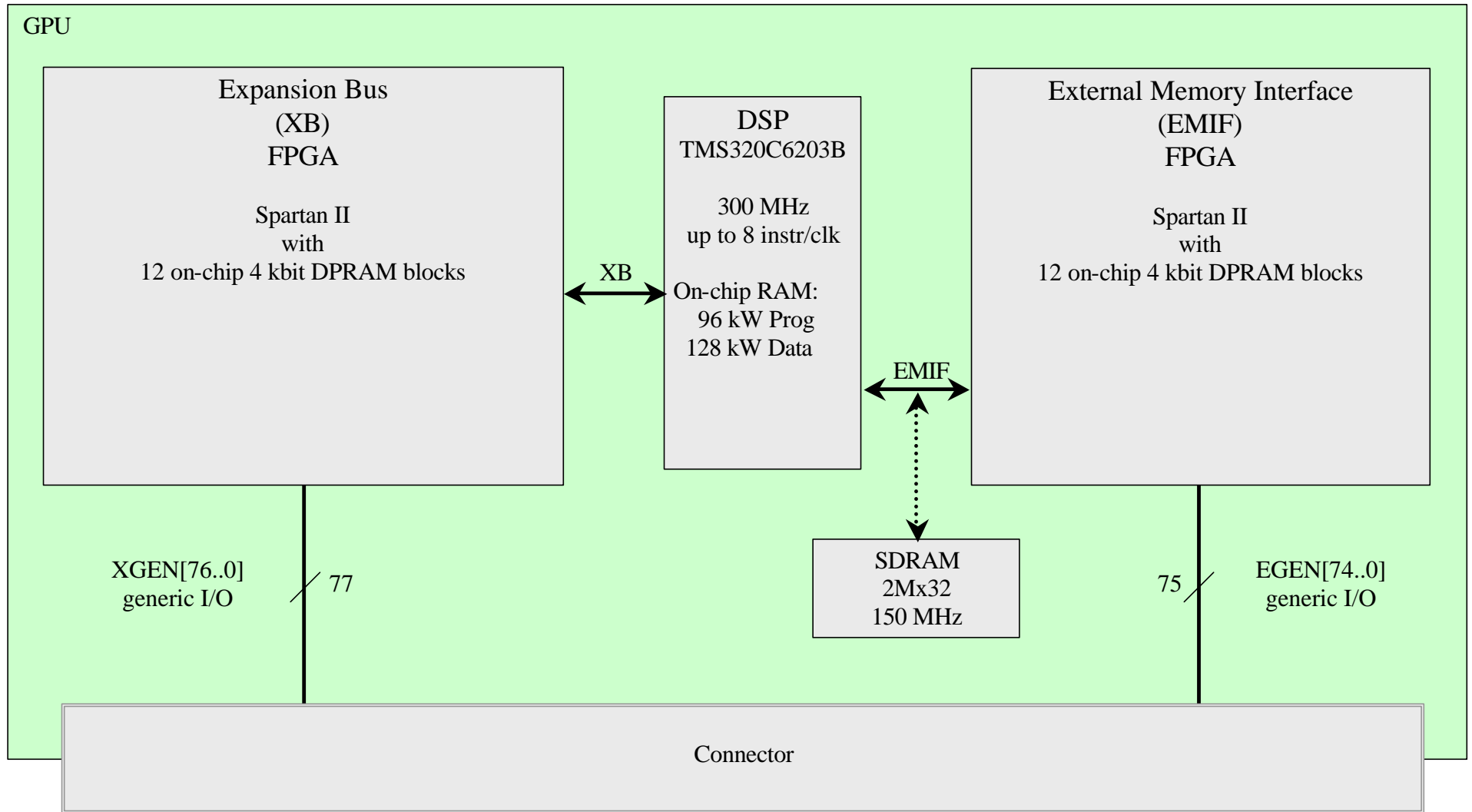
Tx = XC2VP2 FPGA utilizing four MGT serializers.  
 Rx = XC2VP2 FPGA utilizing four MGT deserializers.  
 Mx = XC2VP2 FPGA Master FPGA, no MGT's used.

TXRX: Tx's and Rx's are related, because Rx needs SCA info and Tx needs lock info.  
 Tx: one spare fiber per chamber—can be used for CAL.  
 Rx: two spare fibers per chamber—can be used for current monitoring.

# ROD Subsystems



# Generic Processing Unit (GPU, HPU, DPU, SPU, RPU)



## Statistics

size	< 70 mm x 70 mm
power	< 3 W
data BW	>50 Mword/s XB + >50 Mword/s EMIF
cost	~\$250.00 each excluding NRE, qty 350
status	24 production samples in hand

## Abbreviations

GPU	Generic Processing Unit
HPU	Host Processing Unit
DPU	Data Processing Unit
SPU	S Data Processing Unit
RPU	R Data Processing Unit

## ROD Verilog Coding Summary

Abbreviation	Type	Qty.	Loc.	Coded ?	Tested ?	Final ?	Final Complexity	Major Functions
Flash	CPLD	1	RMB	yes	√√√	yes	3	Interfaces flash memory to HPU and VME. Manages ROD startup.
Host	CPLD	1	RMB	yes	√√√	yes	2	Generates various motherboard control signals.
Noisy	CPLD	1	RMB	yes	√√√	yes	2	Controls clock generation subsystem.
Quiet	CPLD	1	RMB	yes	√√√	yes	2	Controls clock generation subsystem.
VMEC	CPLD	1	RMB	yes	√√	yes	4	Controls VME interface.
VMED	CPLD	1	RMB	yes	√√	yes	2	Manages VME data flow.
HPU XB	FPGA	1	HPU	yes	√√√	yes	4	Interfaces DSP to DPU Control.
HPU EMIF	FPGA	1	HPU	yes	√√√	yes	1	Interfaces DSP to busses on motherboard.
DC	FPGA	1	RMB	yes	√√√	yes	5	Manages DPU Control data flow.
DPU XB	FPGA	12	DPU	yes	√√	yes	5	Interfaces DSP to DPU Control. Receives and buffers raw detector data.
DPU EMIF	FPGA	12	DPU	yes	√	no	3	Interfaces DSP to Data Exchange.
BPI	FPGA	6	RMB	yes	yes	no	3	Receives and buffers raw detector data. Forwards raw data to DPU's.
TTC	FPGA	1	RMB	yes	yes	no	4	Interfaces HPU to ATLAS TTC. Generates SCA control stream (for SIT only).
DXF	FPGA	2	RMB	yes	no	no	4	Manages Data Exchange data flow.
DXB	FPGA	1	RMB	no			2	Merges DX (event) data from ROD halves. Forwards DX (event) data to ROL.
TMMX	FPGA	1	CTM	no			3	Interfaces HPU to CTM.
TMRX	FPGA	6	CTM	no			4	Buffers/reformats GLink data from detector.
TMTX	FPGA	3	CTM	no*			4	Generates SCA control stream.

\*: SCA controller Verilog has been coded and extensively tested in the SIT.

SIT: System Integration Tests

Qty.: Number of chips using identical Verilog code per ROD slot.

RMB: ROD motherboard.

CTM: Final CSC Transition Module.

Final: yes = no major changes to functionality are expected for deployment in ATLAS.

no = changes to functionality are expected, either because of code inadequacies or code incompatibility with the CTM.

Final Complexity: 1 = lowest complexity, 5 = highest complexity

Tested: no = not tested, √ = minimally tested, √√ = moderately tested, √√√ = extensively tested. All tests were performed with working hardware.

## ROD Bus Performance

Rate	ROD max	CSC burst	CSC average	Unit	W =	Note
Interconnect / CTM clock (RCLK) rate:	> 80	80	80	MHz		1
Interconnect / CTM data rate:	80	71	64	MW/s per DPU	16 bits	2
Interconnect rate to DPU's:	70	48	43	MW/s per DPU	25 bits	
SPU expansion bus rate, data:	75	48	43	MW/s per SPU	32 bits	3
DPU expansion bus rate, DPU Control:	20		< 1	MW/s per DPU	32 bits	3
SPU EMIF data rate (e.g., data to RPU):	75		< 2	MW/s per SPU	32 bits	4
RPU EMIF data rate (e.g., data from SPU, data to ROL):	75		< 20	MW/s per RPU	32 bits	
Data Exchange front-side data rate:	50		< 20	MW/s per half-ROD	32 bits	5
Data Exchange / CTM clock (DCLK) rate:	70	40	40	MHz	32 bits	
Data Exchange / CTM data rate:	70		< 20	MW/s per ROD	32 bits	
DPU Control total bandwidth:	50		< 10	MW/s per ROD	32 bits	6

Notes:

CSC burst and average rates assume the worst-case scenario of 100 kHz L1A with no overlapping timeslices.

1. The CTM derives RCLK from the bunch crossing clock distributed by the TIM. Though Virtex FPGA's have some frequency multiplication and division capabilities, the most practical frequency to use is twice the bunch crossing frequency.
2. Wider paths are possible if fewer than 12 DPU's are serviced by the Interconnect subsystem.
3. Data and DPU Control share the DPU's expansion bus. For CSC, the average data rate is 43 MW/s (@100 kHz L1), which is transferred across the expansion bus in 75 MW/s bursts. This leaves ~10 MW/s of average DPU Control bandwidth.
4. The rate listed is for precision SPU's. Transverse SPU's will have higher data rates, because the transverse SPU handles data from all four layers. This is accounted for in the rates listed for RPU EMIF and Data Exchange. For details, see "Data Exchange Details, Continued".
5. Each Data Exchange front side FPGA supports six DPU's. The front-side FPGA can transfer data between its DPU's as well as to the back side (which will send the data to the ROL on the CTM).
6. DPU Control is used for initialization and monitoring. It may also be used for coordinating data transfer on a per-event basis.

## ROD Signal Integrity: Overview

GPU				
Signal Class	Termination	Loads	Simulation	Workaround if Problem
DSP data busses	none	1 (xb) 2 (emif)	IBIS	reduce CPU clock rate (SDRAM) increase bus delays (writes to FPGA's) change driver slew rate (reads from FPGA's)
DSP address busses	none	1 (xb) 2 (emif)	IBIS	reduce CPU clock rate (SDRAM) increase bus delays (access to FPGA's)
SDRAM control	none	1	IBIS	reduce CPU clock rate (SDRAM)
DSP clock and strobe outputs	series	max 2	IBIS	change value of series termination resistors

Motherboard				
Signal Class	Termination	Loads	Simulation	Workaround if Problem
FPGA busses	none	6	IBIS	reduce driver slew rate; reduce clock rate
Spartan II FPGA pt-to-pt	series	1	IBIS including crosstalk	reduce driver slew rate; reduce clock rate
Virtex FPGA pt-to-pt (CTM-to-ROD)	series (Virtex DCI)	max 2	none	change driver impedance via Virtex's DCI change data phase via Virtex's DLL change receiver threshold via Spartan's VREF **
LVDS	differential	1	none	change value of differential termination resistor
non-PLL clock drivers	series (R packs)	* max 8	IBIS	change value of series termination resistors
PLL clock drivers	series (integrated)	max 4	IBIS	none

### GPU Notes:

1. The SDRAM clock rate is always one-half of the CPU clock rate.
2. Timing analysis predicts a max within-spec SDRAM clock rate of 290/2 MHz.
3. SDRAM use is optional for ATLAS. The SDRAM has proven useful in various tests, including the SIT.
4. The timing parameters of DSP bus cycles that asynchronously access the FPGA's can be set by software. For example, when running at 300 MHz, the width of the write strobe can be adjusted in 3.33 ns increments.
5. Spartan II driver slew rate and drive strength are determined by the FPGA configuration.

### Motherboard Notes:

1. Except for LVDS traces, all traces are long enough to be considered transmission lines.
2. LVDS traces on the ROD motherboard are very short.
3. Virtex driver impedance can be set by DCI (Digitally Controlled Impedance), which matches driver impedance to two precision resistors per output bank. The impedance range is 20-100 ohms.
4. Spartan II driver slew rate and drive strength are determined by the FPGA configuration.

\* At most four GPU's (eight FPGA's) share a single configuration clock.

\*\* 1% resistors set VREF to 1.25V, which is ideal for receiving the CTM's 0-2.5V output swing.

# ROD Signal Integrity: PLL-Driven Clocks

Clock	Oper MHz	Max MHz	Limited by	Max Stubs	Max Loads	CSC use
HPU_CLK	30	30	DSP	0	1	1/10 CPU clock
DPU_CLK	30	30	DSP	2	2	1/10 CPU clock
DX_CLK	40	50	DX bus settling	2	2	Data Exchange clock
DC_CLK	40	50	DC bus settling	0	* 4	DPU Control clock
RCLK	80	80	FPGA logic	2	** 4	CTM → Interconnect data transfer clock
SCLK	60	70	FPGA logic	2	2	Interconnect → DPU data transfer clock
TCLK	40	40	VCXO on CTM	2	2	ATLAS/LHC TTC clock
DCLK	40	40	S-LINK	0	1	Data Exchange → S-LINK data transfer clock
DXINT_CLK	50	70	DX FIFO / DX FPGA's	0	1	Data Exchange internal (front→back) clock
VME_CLK	40	60	VME FIFO / VME PLD	0	1	VME interface clock

## Notes:

1. Oper MHz = the anticipated operating rate for the CSC ROD.
2. Max MHz = the maximum rate at which the hardware could operate.
3. The operating range of the PLL clock drivers on the ROD motherboard is 25 to 125 MHz.
4. Termination is integrated series termination at the PLL clock driver.
5. For phase-critical clocks, loads are matched, in some cases with dedicated load capacitors.
6. Stubs on the GPU are not considered, because their loads are very close to each other.

\* The GPU has four loads for DC\_CLK.

\*\* The GPU has two loads for RCLK. For CSC, the GPU RCLK's are not used.

## Topology for clocks with two stubs:



# ROD Power

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## Power Sequencing

ROD power can be enabled/disabled by the RCC. \*

Supply voltages are sequenced by a CPLD. \*

No supply voltage is enabled unless both backplane voltages (5V and 3.3V) are valid.

The power system is designed to handle FPGA and DSP power-on surges.

\* Except MB\_VCC and MB\_VCC5, which power the VME interface.

## Power Protection

HPU software can monitor temperature on each GPU and at three locations on the motherboard.

Software can monitor all supply voltages and currents.

Supply voltages are protected from overvoltage by a comparator + SCR circuit.

FET power switches provide the following for all supply voltages:

- current limit,

- overcurrent shutdown (thermal shutdown of power switch),

- soft start.

## Estimated Maximum Power Consumption

3.3V:	14 W/ROD
<u>5V:</u>	<u>36 W/ROD</u>
Total:	50 W/ROD

## ROD Testing

Subsystem	Tests	Not yet Tested
Backplane	exercise of most connections (P0 tested with continuity tester)	80 MHz data transfer from CTM to ROD
Clock Generation	exercise of most clocks at a variety of frequencies	DCLK, DXINT_CLK, DX_CLK, some functionality that is not currently used
Data Exchange (DX)	tests of electrical connectivity (with continuity tester)	no operational testing
DPU Control	extensive automated tests, extensive exercise in SIT	simultaneous DC and IC operation
Front Panel	exercise of many features	
DPU's	max of six DPU's simultaneously installed	operational testing of GPU → DX
Host (HPU)	extensive exercising	HPU ← → DX
Interconnect (IC)	extensive exercising in SIT and beam tests	reception of CTM data at 80 MHz
JTAG	used to program CPLD's, used to communicate with DSP's via emulator	optional boundary scan paths
Power	exercise of: all voltages, power sequencing, power monitoring, current limiting circuitry, overvoltage protection	motherboard fully loaded with 13 GPU's
VME Interface	extensive exercise, tests with automated test software	block transfers, transfers via VME FIFO, Configuration ROM (CR Flash) Control/Status Registers (CSR)
(GPU)	extensive automated tests using standalone GPU Test Board, exercising in role of HPU, exercising in role of SPU	some functionality that is not currently used, e.g., serial number chip

# ROD Performance at the System Integration Test

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The ROD was equipped with Verilog specifically designed to support the SIT. Details are in Reference 5.

In some ways SIT ROD behavior is like ATLAS ROD behavior:

SCA controller:

- generates an SCA control stream suitable for ATLAS running at 100 kHz L1 rate
- can read out any number of timeslices per trigger (subject to intrinsic limitations)

Handling of timeslices shared by two or more triggers:

- each timeslice is read out from the ASMMI once and only once
- the first timeslice of each trigger is marked with a flag
- DPU software uses the flag to supply its processing algorithm with complete trigger data
- the sharing of timeslices is transparent downstream from the SPU's input buffer

Handling of link loss-of-lock:

- hardware automatically re-establishes lock
- data quantity to DPU's is independent of link lock, invalid timeslices are flagged

Recording of system status information on a per timeslice basis, e.g.:

- link status (link-detected bit errors, loss of lock, unexpected DAV, etc.)
- SCA cell address
- SCA controller status (e.g., fault if the capacitor reserve is exhausted)

The DPU is running a prototype version of the final DPU software framework:

- Input buffer behavior and performance are the same as in ATLAS at 100 kHz L1 rate

**The ROD accepts data at the maximum ASMMI output rate**

In some ways SIT ROD behavior is not like ATLAS ROD behavior:

ATLAS L1 trigger rules enforcement—in ATLAS these rules are enforced by the L1 CTP

- fewer than eight L1's in 80 microseconds
- four BC dead time following each L1

Storage of data in DPU SDRAM (8 Mbyte/DPU) during run

Readout of data after run:

DPU → DPU Control Subsystem → HPU → VME

The DPU is running a prototype version of the final DPU software framework:

- Output buffer contents are DMA'd to SDRAM rather than to the EMIF FPGA
- Output buffer data rate is ~2/20 times higher than in the ATLAS RPU/SPU at 100 kHz

DPU data processing is not the same as ATLAS RPU/SPU data processing

Intrinsic System Limitations:

The SCA contains 144 capacitors per channel.

In ATLAS, ~70 capacitors are required for trigger latency pipelining.

In ATLAS, ~32 capacitors at most can be simultaneously awaiting readout.

ASMMI readout time is ~2 microseconds per timeslice.

At most four timeslices per trigger can be read out at 100 kHz L1 rate.

Analysis of SIT runs:

System status information from several cosmic runs showed zero errors in 5.7 hours of running.

System operation was demonstrated at 106 kHz trigger rate:

- the 8/80 L1 rule was increased to 10/80 in order to allow the high trigger rate
- four timeslices were read out per trigger

## ROD Production Runs

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<b>Run</b>	<b>Qty</b>	<b>Delivery</b>	<b>Comment</b>
GPU Short	26	19-Mar-04	Some quirks but otherwise excellent yield.
GPU Long	330	TBD	Thirteen GPU's per ROD: $330/13 = 25.4$
Motherboard Short	5	ASAP	Quoted. Ready to place order.
Motherboard Long	20	TBD	Sixteen plus four spares.

The lead time for assembly runs is six weeks or less.

## Summary

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Several GPU's:

extensively tested and exercised since January 2001.

One ROD motherboard:

gradually assembled, tested and exercised since September 2001.

System Integration Tests:

were completed in 2004

one prototype ROD motherboard

five production GPU's

one prototype transition module (TTM, not suitable for ATLAS)

four ASMII's + ASMI's and chamber

Short production runs will precede final production runs.

The GPU short production run was completed with excellent yield.

The motherboard short production run is quoted.

Some final ROD tests will be performed after the motherboard short run.

# Nomenclature

## ATLAS

RCC	Rod Crate Controller. A COTS single-board computer that is the ROD Crate VME master.
ROB	Readout Buffer. The ATLAS-standard module that receives and buffers event data from the ROD.
ROD	Readout Driver.
ROL	Readout Link. The ATLAS-standard data link that transports event data from the ROD to the ROB.
TIM	Timing Interface Module. A module in the ROD crate that receives TTC signals and distributes them to the ROD's. This module was designed at UCL and is used by several ATLAS subdetectors.

## ATLAS CSC

ASM	Amplifier-shaper Module. Module mounted on the chamber that converts analog chamber signals to the digital stream that is transmitted to the ROD. There are now two separate boards that together perform this function, ASM I, and ASM II.
ASM I	The ASM that actually contains the amplifier-shaper chips.
ASM II	The ASM that contains the SCA's, A/D's, G-Links, etc.
SCA	Switched Capacitor Array. The analog pipeline in which amplified and shaped chamber signals are stored until readout.

## UCI Hardware for ATLAS CSC

BPI	Backplane Interface. A type of FPGA in the ROD's Interconnect subsystem.
CRB	CSC ROD Backplane. The custom P5/P6 backplane that supplies power to the ROD's and TM's, carries TTC signals from the TIM to ROD slots, and carries signals between each ROD and its TM.
DC	DPU Control. The ROD subsystem that provides the HPU with access to the memory space of the DPU's.
DX	Data Exchange. The ROD subsystem that manages data transfers between SPU's and RPU's and between RPU's and the ROL.
GPU	Generic Processing Unit.
HPU	Host Processing Unit. The GPU on the ROD that controls most of the ROD, including the DPU's.
DPU	Data Processing Unit. Any GPU on the ROD that is not the HPU.
SPU	S Data Processing Unit. A DPU that receives and sparsifies raw chamber data. Each ROD has ten SPU's, five per chamber.
RPU	R Data Processing Unit. A DPU that receives and further processes sparsified data. Each ROD has two RPU's, one per chamber.
TM	Transition Module. The circuit board that resides in the slot behind each ROD slot.
TTC	Timing Trigger and Control. Refers to the ATLAS clock and control distribution system. Also, the name of an FPGA in the ROD's Interconnect subsystem.
TTM	Test Transition Module. A prototype transition module designed specifically for use in the 2002 Joint Tests.

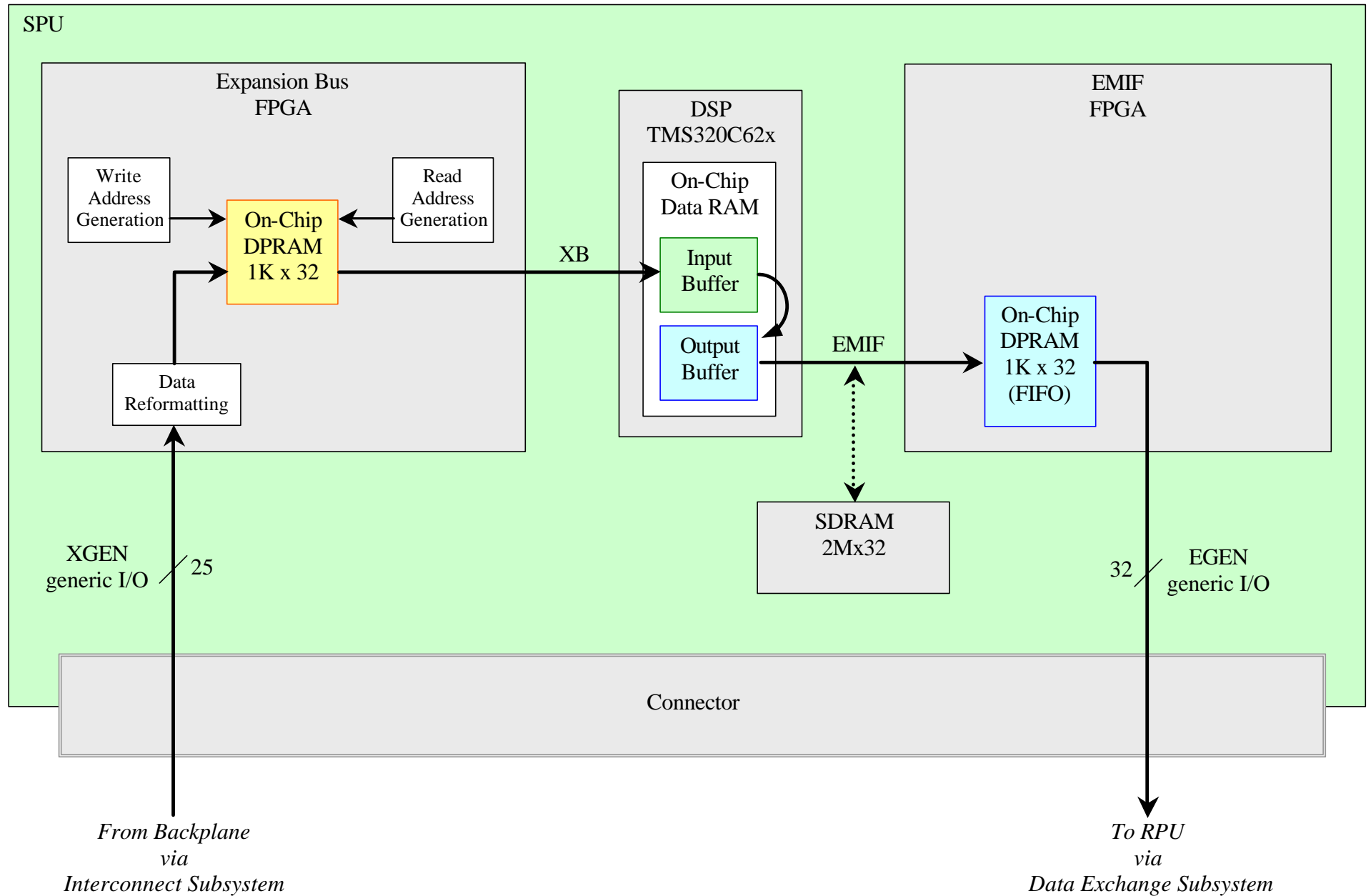
## ROD Subsystems

Name	Abbreviation	Description
Backplane	BK or Back	Contains backplane connectors, including standard VME and custom P5/P6.
Clock Generation	CG	Generates most clocks on the ROD.
Data Exchange	DX	Provides for data transfer among GPU's as well as to the ROL.
DPU Control	DC	Provides the HPU with access to the memory space of all DPU's.
Front Panel	FP or Front	Contains various connectors, switches, and indicators located on the ROD front panel.
Half ROD	Half	Contains six DPU's. There are two instances of this subsystem: A and B.
Half A	A	Contains six DPU's.
Half B	B	Contains six DPU's.
Host	HO or Host	Contains the HPU as well as chips to interface the HPU to the remainder of the ROD.
Interconnect	IC	Provides data routing among the DPU's and the backplane. Also generates SCA control signals.
JTAG	JT or JTAG	Routes boundary-scan signals used for in-system device programming and DSP emulation.
Power	PW or PWR	Generates, switches, and measures voltages. Also protects against overcurrent and overvoltage.
VME Interface	VM or VME	Interfaces the ROD to VME.

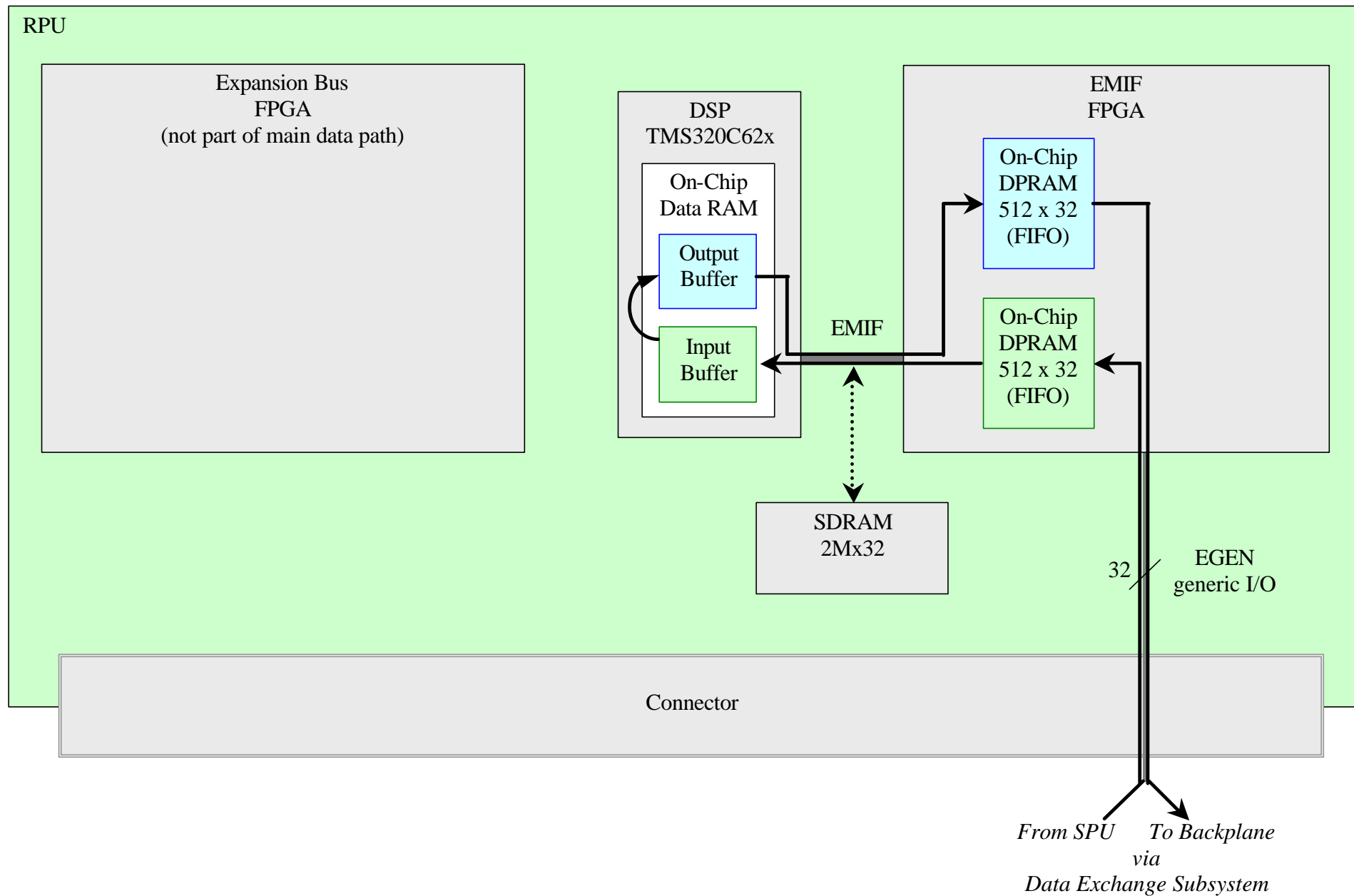
## General

CPLD	Complex Programmable Logic Device. A type of programmable chip that retains its programming regardless of whether power is applied.
DSP	Digital Signal Processor. A microprocessor characterized by high processing efficiency, high on-chip memory bandwidth, low power, low cost, etc.
EMIF	External Memory Interface. One of the two data busses on the TMS320C6203 DSP. See also XB.
FPGA	Field Programmable Gate Array. A type of programmable chip that must be programmed every time power is applied.
JTAG	Joint Test Action Group. Refers to IEEE 1149.1 standard for boundary scan. This standard is also used for Xilinx CPLD in-system programming and Texas Instruments DSP in-system emulation.
XB	Expansion Bus. One of the two data busses on the TMS320C6203 DSP. See also EMIF.

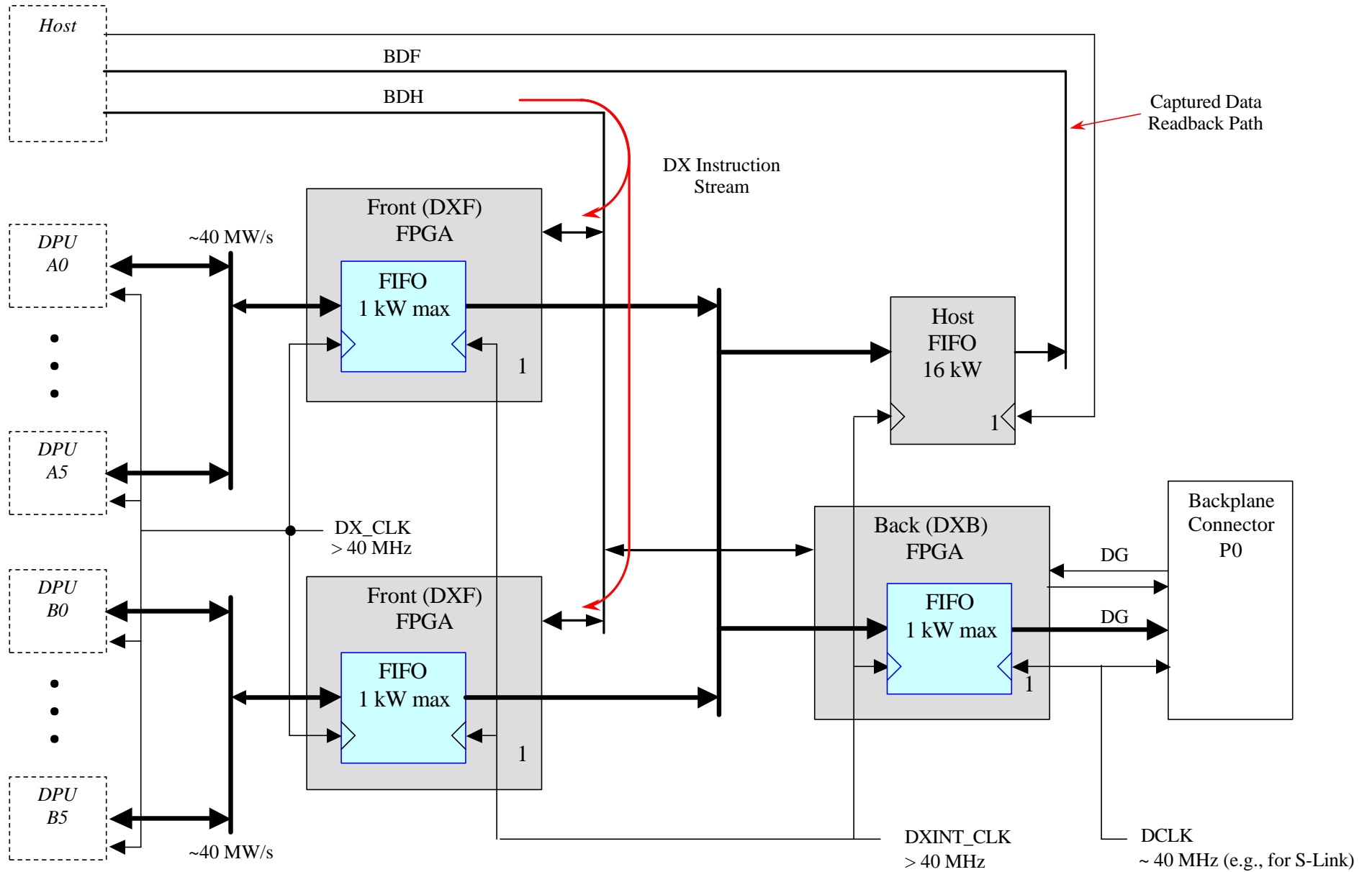
# Main Data Paths of the SPU



# Main Data Paths of the RPU

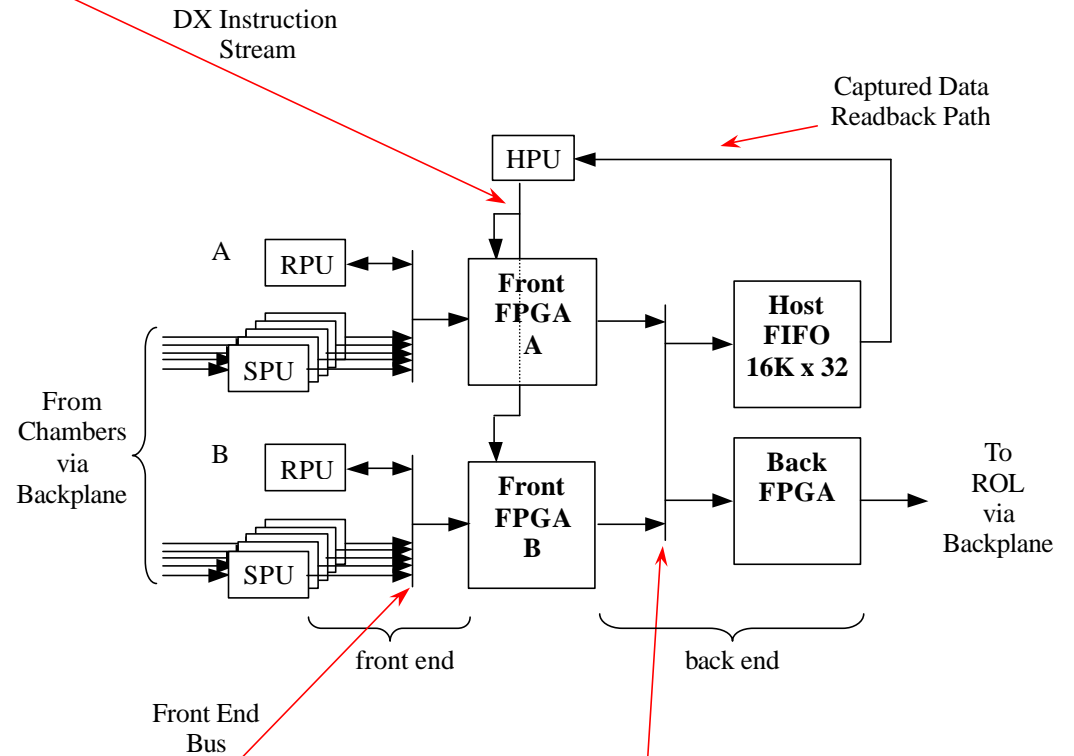


# Data Exchange (DX) Details



## Data Exchange Details, Continued

Side	DX Instruction Stream	Word Count
	<b>Build Sparsified Event: SPU's ® RPU</b>	
A and B	run front sequence: SPU's → RPU source: SPU0, SPU1, SPU2, SPU3, SPU4 destination: RPU	1
	<b>Build Final Event: RPU's ® Back End</b>	
A	write control word to back end: 0xb0f00000 (beginning of fragment)	1 +1
A	write leader to back end: CSC ROD leader	1 +8
A and B	run front sequence: RPU's → back end source: RPU destination: back end	1
A	write command word to back end: release DX Internal Bus (release it to B)	1 +1
B	write trailer: CSC ROD trailer	1 +3
B	write control word to back end: 0xe0f00000 (end of fragment)	1 +1
B	write command word to back end: Release DX Internal Bus (return it to A)	1 +1
	<b>total</b>	<b>23 words/L1</b>
	<b>typical HPU DMA rate to DX</b>	<b>2.3 MW/s</b>



DX Front End Bus Streams	Word Count
data from SPU0-SPU4 → RPU	$4*15 + 1*45 = 105$ typ
data from RPU → ROL (1 chamber)	$105 - 6*5 = 75$ typ
<b>typical total</b>	<b>180 words/L1</b>
<b>typical rate</b>	<b>18.0 MW/s</b>

Driver	DX Internal Bus Stream	Word Count
A	CSC ROD leader	1+8
A	data from RPU A (1 chamber)	75 typ
B	data from RPU B (1 chamber)	75 typ
B	CSC ROD trailer	1+3
	<b>typical total</b>	<b>163 words/L1</b>
	<b>typical rate to ROL</b>	<b>16.3 MW/s</b>

Typical values are based on

L1 rate = 100 kHz,

acceptance window = 75 ns,

and these conservative assumptions:

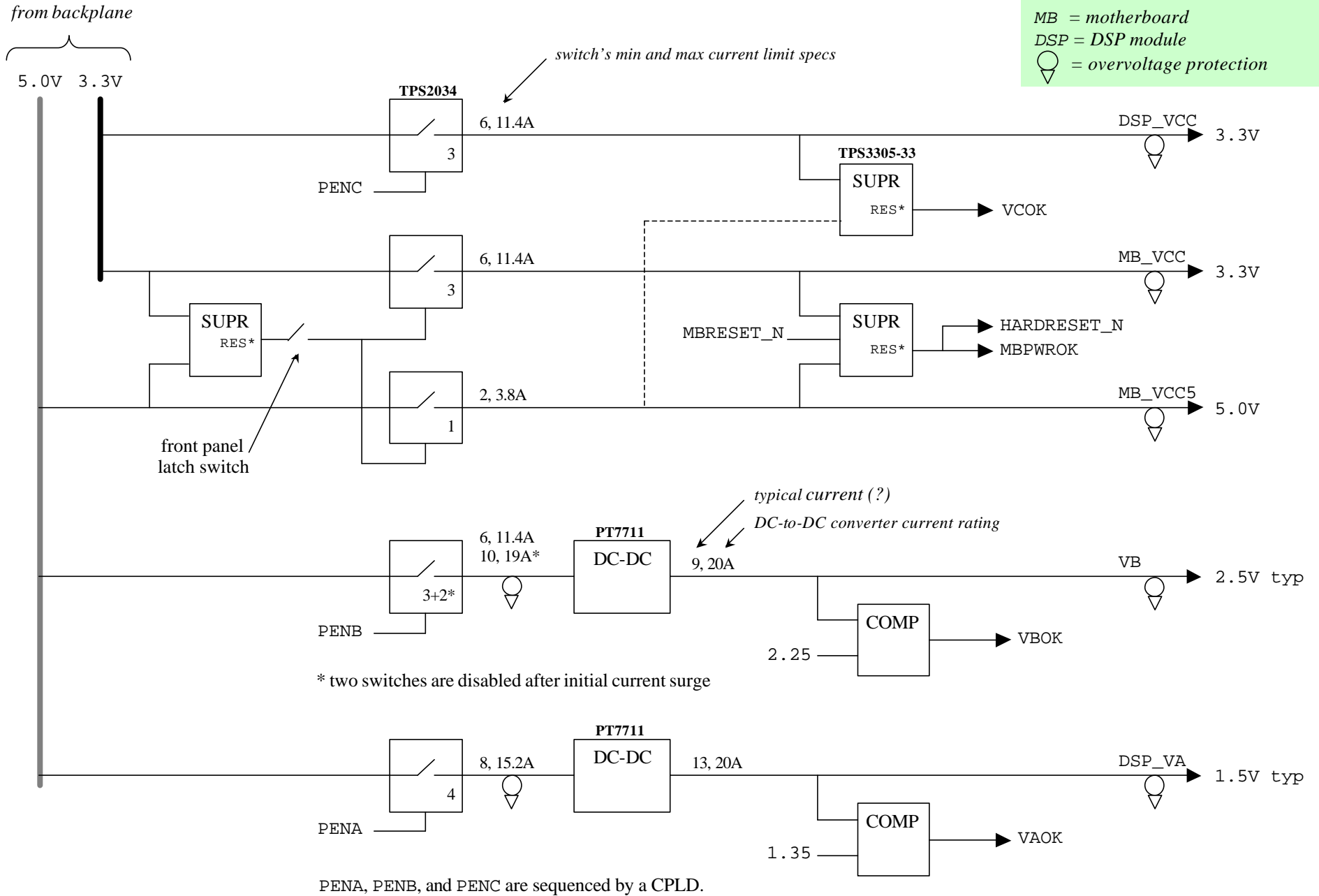
RPU does NOT perform neutron rejection,

RPU does NOT reduce data volume

flux = 1500 Hz/cm<sup>2</sup>,

five channels are read out per hit (three for transverse).

# ROD Power Details



## Transition Module Features

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### *CTM-Specific Features*

Chambers supported:	2	chambers
Data fibers:	20+4	fibers *
Control fibers:	10+2	fibers *
Data stream from ASM2's	32 40	bits/ASM2 MHz, including padding
Data stream to ROD:	16 60-80	bits/SPU MHz
Control stream from ROD:	16 40	bits MHz
Clock phase verniers:	1	per control fiber
Clock phase vernier step:	1.25	ns

\* Spare data fibers can be used for power supply current monitoring.

Spare control fibers can be used for calibration signals, e.g., DAC setting and CAL pulse.

### *System Features*

Data Synchronization:	The ASM connects one bit of its control stream to DAV* on both of its serializers.	
Lock Establishment:	The TM helps establish lock and recovers from loss of lock by transmitting fill frames when data links lose lock.	on a per-ASM basis
Optical Compatibility:	Optical Fibers, Transmitters and Receivers must be compatible.	
Optical Power Budget:	The TM must operate within budgeted optical power limits.	
Laser safety:	The TM disables all transmitters if there is excessive loss of lock. The TM disables all transmitters when the rack door interlock signal is not present.	on a per-TM basis

# Notes for Hardware Overview Slide

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## CSC Readout Electronics Overview

This slide shows the chambers, optical links, and contents of the CSC ROD crate.

ASM P indicates an amplifier/shaper module connected to one layer of precision strips.

ASM T indicates an amplifier/shaper module connected to four layers of transverse strips.

SPU P is a DPU dedicated to sparsifying one layer of precision strips.

SPU T is a DPU dedicated to sparsifying four layers of transverse strips.

RPU is a DPU dedicated to rejecting neutrons hits from one chamber.

HPU is the Host Processing Unit, which orchestrates activity on the ROD.

DX is the Data Exchange subsystem. It moves data from SPU's to RPU's and from RPU's to the Readout Link (ROL).

## ROD Subsystems

**Interconnect:** This subsystem conveys raw chamber data from the backplane to the DPU's. For diagnostic purposes, it can move data from DPU's in one side of the ROD to DPU's in the other side. The Interconnect subsystem contains the TTC FPGA, which receives ATLAS Timing Trigger and Control information from the ROD crate's TIM module. The TTC FPGA provides the HPU with a stream of trigger information, such as trigger type, arrival time, L1ID, and BCID.

**DPU Control:** This subsystem provides the HPU with access to the memory space of all DPU's. The HPU is the master of DPU Control. The DPU's are slaves. During normal running, the HPU uses the DPU Control subsystem to deliver a command stream to DPU's and to read progress information from DPU's. For example, the command stream tells the DPU's to process events. After the events are processed, the HPU may read status information from DPU's (e.g., error counts). A summary of such information may be needed in the status field of each event fragment.

**DPU:** Data Processing Units are DSP modules. They process raw chamber data (SPU's) or sparsified data (RPU's). The DPU's are organized as two groups or half-ROD's. Each half-ROD contains six DPU's, a dedicated DPU Control bus, and a dedicated Data Exchange bus.

**Host:** This subsystem contains the HPU (a DSP module) as well as buffers and logic that allow the HPU to access most resources on the ROD motherboard.

**VME Interface:** This is a slave VME interface. It contains a dual-port RAM for random-access transfers between ROD Crate Controller (RCC) and ROD and a FIFO for burst transfers (ROD → RCC only). The RCC can access a small set of ROD control registers via VME. For example, the RCC can control ROD power and a front-panel LED. If enabled by a front-panel DIP switch, the RCC can read and write the ROD's flash memory, which holds DSP executable code, FPGA configuration streams, etc.

**Data Exchange:** This subsystem transfers data among DPU's, the HPU, and the ROL. The subsystem can sustain a transfer rate on the order of 50 MW/s per half-ROD. A command stream from the HPU controls the Data Exchange. The stream dictates the source(s) and destination(s) for each transfer. The command stream also provides the HPU's contribution to the final ATLAS-standard event fragment (e.g., header, status fields, and trailer).

**Power:** This subsystem controls, sequences, and monitors power and provides over-voltage and over-current protection. The HPU can read out measurements of several voltages and currents.

**Clock Generation:** This subsystem selects clock sources, synthesizes clock frequencies, and distributes clock signals.

The ROD architecture document shows more ROD subsystem details:

<http://positron.ps.uci.edu/~pier/csc/IRODBlockDiagram9.pdf>

## Generic Processing Unit (GPU, HPU, DPU, SPU, RPU)

This slide shows some details of the Generic Processing Unit, which is a DSP+FPGA module. The ROD motherboard accepts 13 GPU's (1 HPU + 12 DPU's). Generic I/O are used according to the GPU's role on the motherboard: HPU or DPU. The ROD Subsystems slide shows XGEN connections on the left side of each GPU and EGEN connections on the right side. FPGA's are configured differently for HPU and DPU. The SDRAM is not needed for final ATLAS running. It is useful for holding simulated data streams during diagnostic tests or for holding raw chamber data during beam tests.

## References

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1. ATLAS CSC Electronics Page:  
<http://positron.ps.uci.edu/~pier/csc/CSCElectronics.html>
2. ROD Architecture Details:  
<http://positron.ps.uci.edu/~pier/csc/IRODBlockDiagram9.pdf>
3. ATLAS CSC Photos:  
<http://positron.ps.uci.edu/~schernau/ROD/pix/>
4. System Power Details:  
[http://positron.ps.uci.edu/~pier/csc/SystemPowerWithMGT\\_01.pdf](http://positron.ps.uci.edu/~pier/csc/SystemPowerWithMGT_01.pdf)
5. SIT-Specific ROD Functionality:  
[http://positron.ps.uci.edu/~pier/csc/CSC\\_TTC\\_and\\_BPI\\_6.pdf](http://positron.ps.uci.edu/~pier/csc/CSC_TTC_and_BPI_6.pdf)
6. ROD Symbolic Netlist:  
<http://positron.ps.uci.edu/~pier/csc/View1.html>