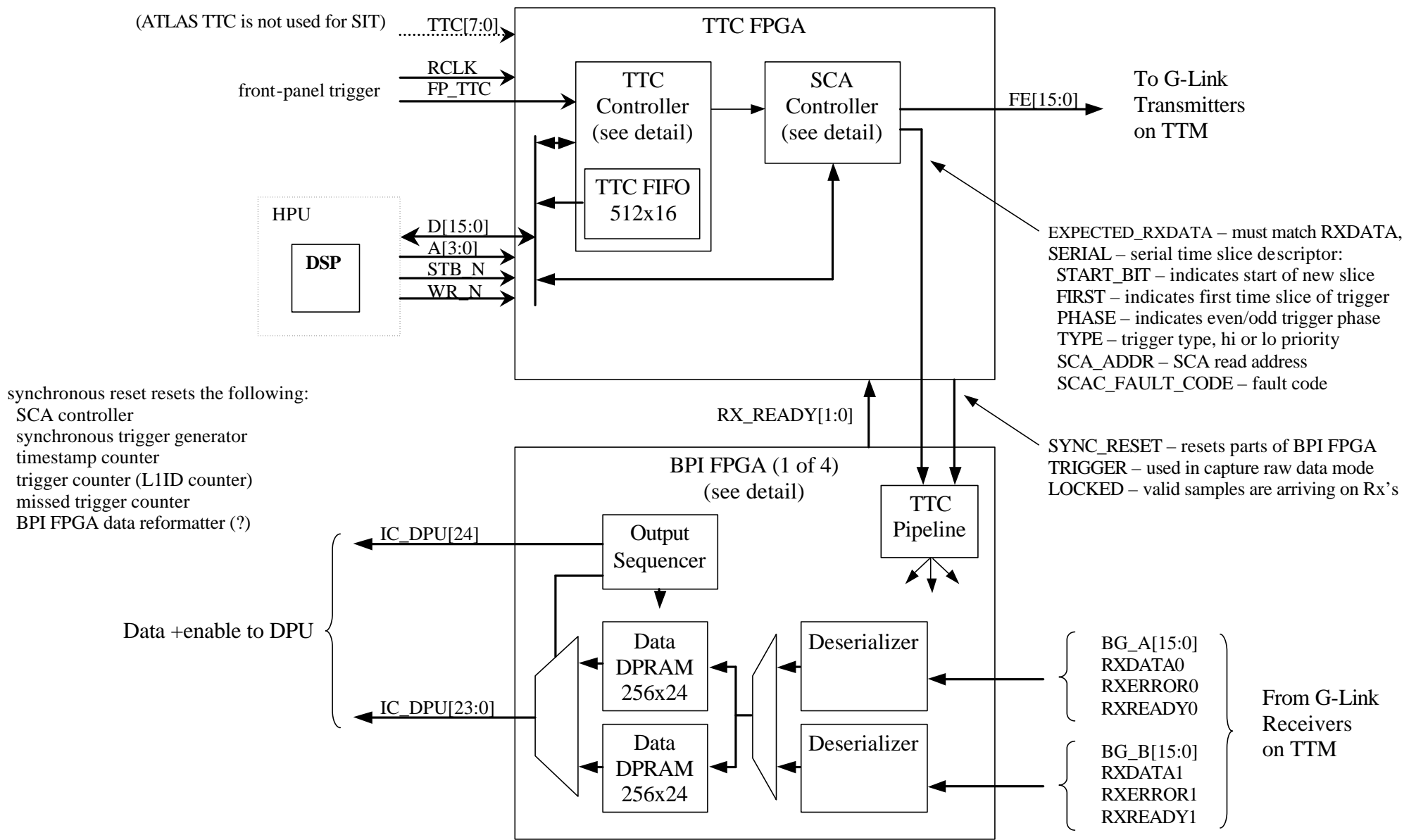
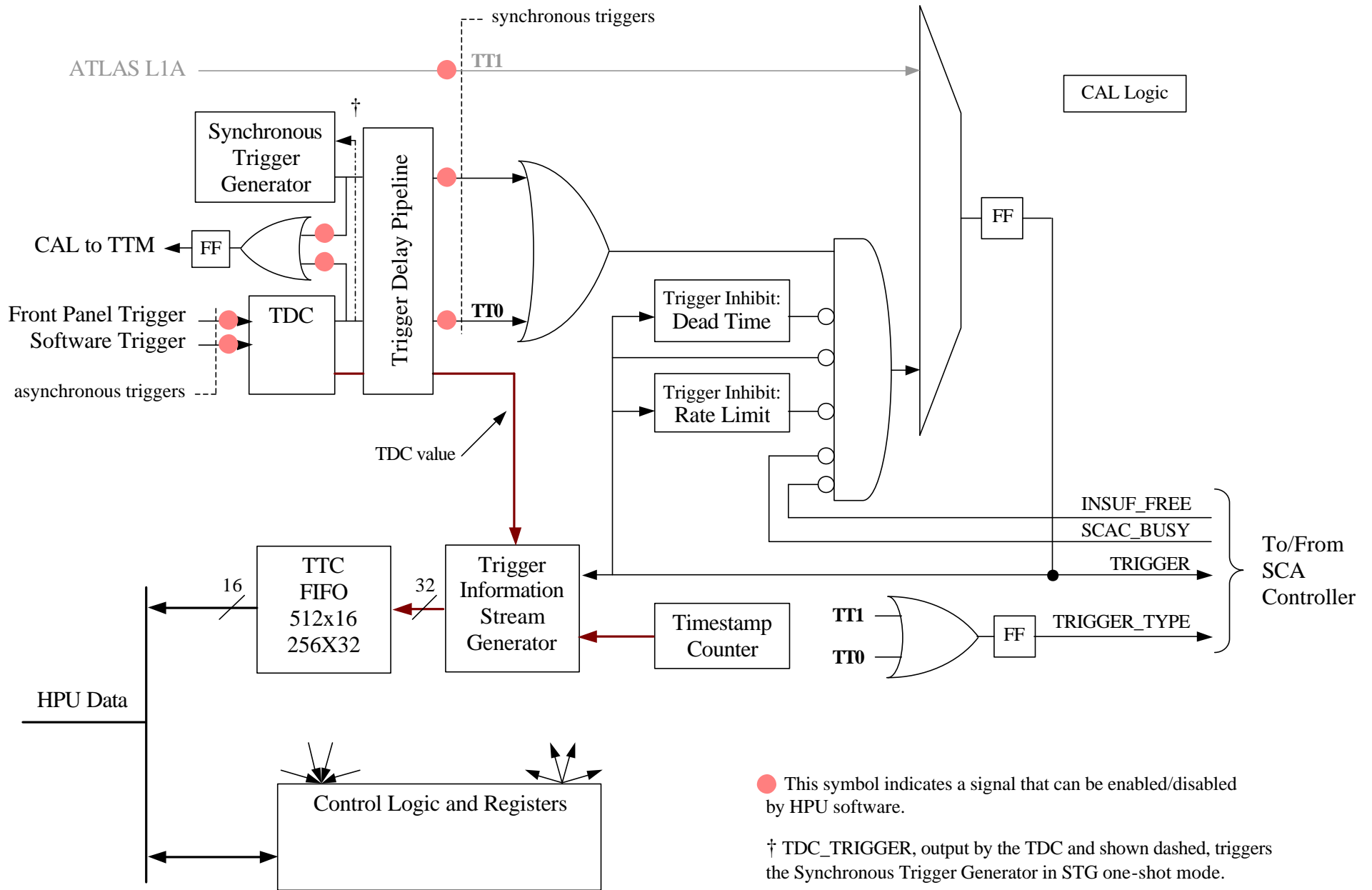


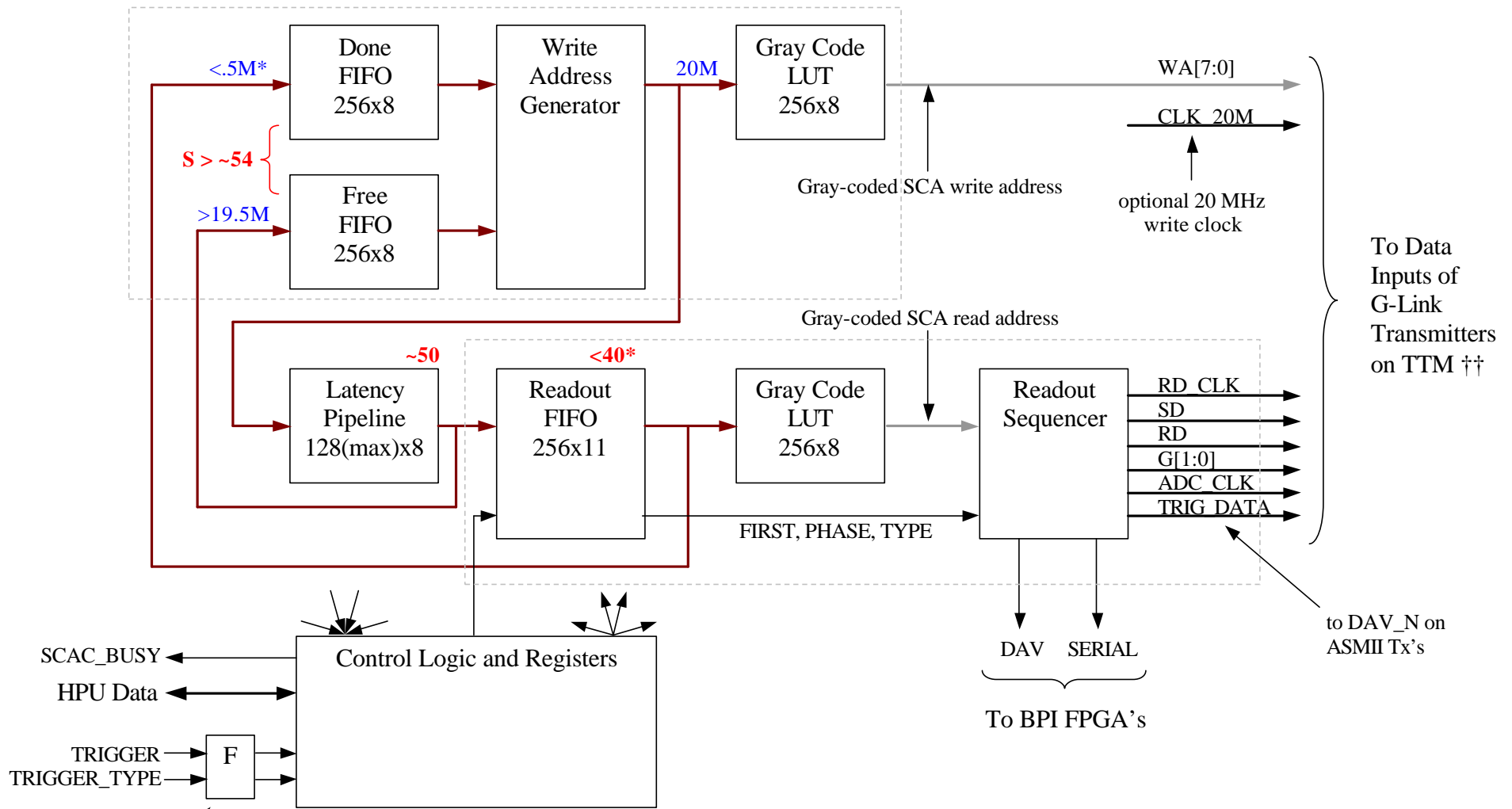
Overview of CSC TTC and BPI FPGA's – System Integration Test Implementation



TTC Controller (TTCC) Detail – System Integration Test Implementation



SCA Controller (SCAC) Detail – System Integration Test Implementation



latency fudge: zero or one clock pipeline, depending on latency setting

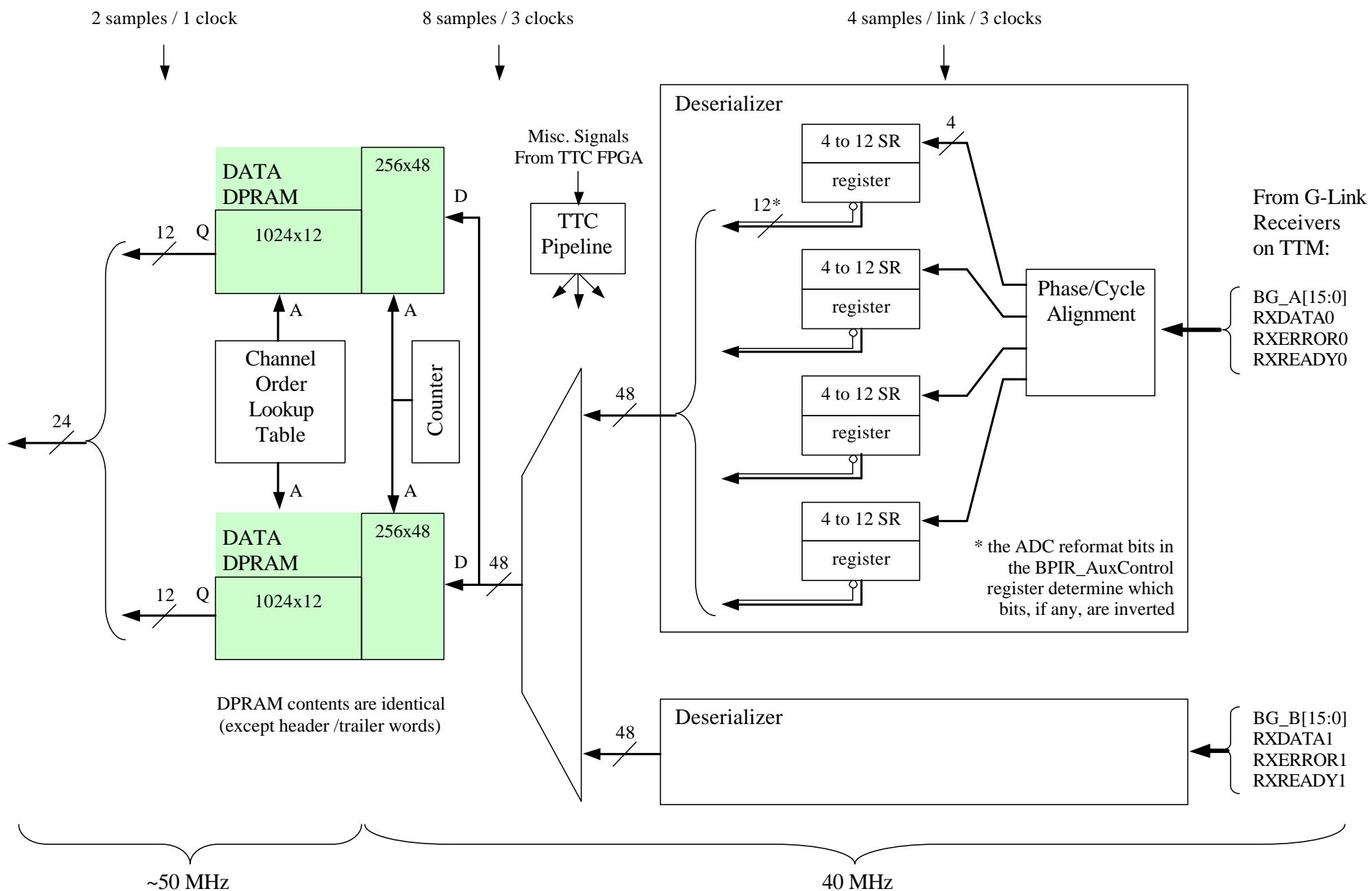
Time to write 144 cells: 7.2 usec
 Time to drain 54 words from Free FIFO: 108 usec
 Ratio: 15
 Time to read out one time slice: ~2 usec

* FIFO occupancy is shown in bold red. Readout FIFO occupancy assumes 8 non-overlapping triggers and 5 samples/trigger.

* FIFO input rates (Hz) are shown in blue. Done FIFO input rate assumes 100 kHz non-overlapping triggers and 5 samples/trigger.

†† Not shown: the SCAC contains a test data generator that when selected drives simulated ASM II output onto the G-Link Tx's.

BPI FPGA Detail – System Integration Test Implementation (many details omitted)



TTC FPGA Registers

Register Name	R/W/S	Address	Contents	Description
<i>In TTC FPGA:</i>				
<i>general:</i>				
TTCR_DLL_Reset	W	0	rrrrrrrrr rrrrrrrr	resets the DLL's, which causes an asynchronous reset until the DLL's lock
TTCR_Status	R	0	UOWFSCDr rrrrrrPRL U = TTCC fault: TTC FIFO underflow O = TTCC fault: TTC FIFO overflow W = SCAC fault: bad SCA write address F = SCAC fault: Free FIFO went empty S = SCAC fault: readout sequencer fault C = BPI supervisor fault – serial cmd collision D = BPI supervisor fault – DAV_N collision P = transition module is not present R = running (MaxTriggers not arrived) L = all enabled data links are locked	miscellaneous fault and status bits: TTC FIFO underflow/overflow results if HPU reads too many/few words from TTC FIFO. Free FIFO going empty indicates insufficient SCA cells, e.g., due to high trigger rate and/or high number of time slices to read out.
TTCR_LinkStatus	R	1	SSSSSSSS RRRRRRRR S = signal detect for each data link R = RXREADY for each data link	
TTCR_Control	R/W	2	PCSNrART EEEEEEEE P = phase align GLink RX C = cycle align GLink RX (must phase align first) S = software trigger N = NOP request A = enable periodic cycle alignment check R = run, else synchronous reset T = enable all Tx's (assert TXDATA) E = enable data link	miscellaneous bits – the E bits determine whether a link's RXREADY should be considered when establishing or reestablishing lock
<i>for TTC controller:</i>				
TTCR_TTCC_Fifo	R	3	VVVVVVVV VVVVVVVV	output of TTC FIFO – see format under Trigger Information Stream Format, below
TTCR_MissedTriggers	R	4	VVVVVVVV VVVVVVVV	number of missed triggers since last synchronous reset, saturates at 0xffff
TTCR_Triggers	R	5	VVVVVVVV VVVVVVVV	number of triggers since last synchronous reset, excluding missed triggers—this value is the least significant halfword of the 32-bit LIID counter or 0xffff if the most significant halfword of the LIID counter is nonzero
TTCR_TTCC_Setup	R/W	6	CcSNFTGL I1111111 Cc = CAL enables: C = 1 → TDC triggers contribute to CAL c = 1 → STG triggers contribute to CAL S = stop (inhibit triggers) after TTCR_MaxTriggers N = on STG trigger, do not increment LIID or queue trigger in TTC FIFO F = enable front panel trigger (must also set T) T = enable TDC trigger (front panel or software) G = enable STG trigger L = enable LIA trigger I = inhibit trigger when insufficient free SCA cells l = max number of triggers allowed within 80 usec	miscellaneous bits CAL enables are independent of trigger enables
TTCR_DeadTime	R/W	7	VVVVVVVV VVVVVVVV	dead time between triggers – after each trigger, subsequent triggers will be inhibited for V+1 clocks (includes effect of TRIGGER flip-flop)
TTCR_MaxTriggers	R/W	8	VVVVVVVV VVVVVVVV	max number of triggers allowed after each synchronous reset (if S==1 in TTCR_TTCC_Setup)
TTCR_TriggerDelay	R/W	9	rrrrrrrrr VVVVVVVV	Length of trigger delay pipeline, which affects only TDC and STG triggers.

TTC FPGA Registers (continued)

<i>for synchronous trigger generator:</i>				
TTCR_STG_Period	R/W	10	VVVVVVVV VVVVVVVV	Burst period, i.e., the number of clock cycles between the first trigger of one burst and the first trigger of the next burst. In one-shot mode this register contains one plus the number of clock cycles between the TDC trigger and the first trigger of the burst. See diagram in notes.
TTCR_STG_Burst	R/W	11	ONNNNNNN IIIIIIII O = one-shot mode N = number of triggers in the burst I = interval between triggers within burst	Burst characteristics. In one-shot mode , the STG is triggered by the TDC output, regardless of the value of the T bit (TDC trigger enable) in the TTCR_TTCC_Setup register.
<i>for SCA controller:</i>				
TTCR_SCAC_Setup	R/W	12	TTLWWRPS ssssssss Tx mode: 00 = drive Tx with SCA control 01 = drive Tx with test pattern 10 = drive Tx with simulated ASMI data 11 = reserved L = reset lookup table address register W = write rate: 00 = 20 MHz, CLK_20M toggled, 0 phase 01 = 20 MHz, CLK_20M toggled, 180 phase 10 = 20 MHz, CLK_20M held low 11 = 40 MHz, CLK_20M held low R = read clock rate: 0 = 5 MHz, 1 = 6.67 MHz P = read clock phase w.r.t. write addresses S = enable simultaneous read/write s = number of time slices to read out per trigger	SCA Controller setup: To reset the lookup table address register, TTCR_GrayLUT must be read while L is set—see >>> notes in sit_scac.v. See note below for Tx test modes. CLK_20M is a GLINK data line that can be selected via jumper on the ASM II to drive the SCA WCK. Phase of WCLK is with respect to write address changes.
TTCR_ROSEQ_Setup	R/W	13	rAAArDDD GrTTTTT A = ADC clock phase w.r.t. RDCLK D = SD phase w.r.t. RDCLK G = LUT select – see TTCR_LUT T = additional delay (min = 2) for TRIG_DATA	Readout sequencer setup. SD is the SCA read address serial data. TRIG_DATA becomes DAV_N for ASMI transmitters. All phases are in RCLK periods (25 ns).
TTCR_LatencyCells	R/W	14	LLLLLLLL CCCCCC L = depth of latency pipeline in clock cycles C = number of SCA cells to use	depth of the latency pipeline, number of SCA cells to use
TTCR_LUT	R/W	15	rrrrrrrr VVVVVVVV	Data to/from lookup tables: gray code LUT (G == 1) readout sequencer LUT (G == 0) G is in TTCR_ROSEQ_Setup. The address is incremented after each access and reset by L bit in TTCR_SCAC_Setup.

See notes on next page.

Notes:

r = reserved
V = binary value

Missed triggers are those that were inhibited due to dead time enforcement, trigger rate enforcement, etc.

Atlas trigger rules:

T triggers in 80 microseconds, max → “Currently, the baseline is to have less than 8 L1A within 80 μs.”
K clocks between triggers, min → “After each L1A a 4 BC dead-time is introduced by the CTP.”

Tx: “Tx” means the TTM’s Glink transmitter (serializer + laser).

Tx mode 01: Tx is driven with 0x0001, 0x0002, 0x0004, 0x0008, ..., 0x4000, 0x8000, 0x0001, 0x0002 ...

Tx mode 10: This mode is intended for use with a loopback fiber(s) between TTM Tx(s) and TTM Rx(s) and with the BPI input sequencer mode set to normal (see BPIR_Control). In this case the DPU(s) will receive simulated ASMI data such that each data halfword arriving at the DPU has the following format:

0000TTTTCCCC0AMM:

bits	range	description
TTTT	0-15	Zero for the first time slice, incremented for each subsequent time slice.
CCCC	0-11	The SCA channel. Each SCA has 12 channels.
A	0-1	The ASMI ADC that converted the data. Each ADC services one SCA.
MM	0-3	The ASMI mux chip that carried the data—this corresponds with the GLink nybble that carried the data (0→Glink bits 0-3, 1→ Glink bits 4-7, etc.) Each mux services two ADC’s.

Data are transmitted on the GLink in triplets:

MSN			LSN	description	increment
0A11	0A10	0A01	0A00	0AMM, A is the same for all nybbles	A toggles every triplet
CCCC	CCCC	CCCC	CCCC	SCA channel: same for all nybbles	CCCC increments every other triplet
TTTT	TTTT	TTTT	TTTT	time slice: same for all nybbles	TTTT increments every time slice *

* The actual value transmitted is T*T T T (the MSB of TTTT is inverted). The deserializer in the BPI FPGA undoes this inversion such that the halfwords arrive at the DPU in the format shown in the first table above.

Example of STG in **one-shot mode**, PERIOD == 8, BURST_N = 2, BURST_I = 4

```

CLK          _____
TDC_TRIGGER  .----.
STG_PERIOD_CNTR =0====X=8=X=7=X=6=X=5=X=4=X=3=X=2=X=1=X=0=====
STG_BURST_I_CNTR  =====1=====X=4=X=3=X=2=X=1=X=4=====
STG_BURST_N_CNTR  =====1=====X=2=====X=1=====
STG_TRIGGER    _____:----.----.
                |----- PERIOD + 1 -----|--- BURST_I ---|
    
```

BPI FPGA Registers

Register Name	R/W/S	Address	Contents	Description
<i>In BPI FPGA:</i>				
BPIR_DLL_RESET	W	0	rrrr	resets the DLL's, which causes an asynchronous reset until the DLL's lock
BPIR_ChipID	W	1	VVVV	chip identifier. The value is passed to the DPU in the IIII field of status word 61. It has no other effect.
BPIR_Status	R	1	rrTO T = fault: bad serial command from TTC FPGA O = fault: output sequencer overrun	miscellaneous status bits—the T bit indicates a probably hardware fault, the O bit indicates that the output sequencer could not keep up with incoming data rate.
BPIR_LinkStatus0 BPIR_LinkStatus1	R	2 3	LRRP L = AAL phase alignment locked R = RXREADY P = AAL phase	link status
BPIR_FAL_Status0 BPIR_FAL_Status1	R	4 5	LrSS L = FAL cycle alignment locked S = FAL cycle select	cycle (full) alignment status
BPIR_Align	R/W	6	MPmp M/m = link 1/0 manual mode P/p = link 1/0 manual phase	auto-alignment system control bits for links 0 and 1
BPIR_Control	R/W	7	MMrL M = input sequencer mode: 0 = disabled 1 = normal 2 = capture raw data from link 0 * Note 1 3 = capture raw data from link 1 * Note 1 L = reset lookup table address register	miscellaneous bits
BPIR_TTC_LatencyL BPIR_TTC_LatencyH	R/W	8 9	VVVV	depth of TTC latency pipeline
BPIR_InWordCountL BPIR_InWordCountH	R/W	10 11	VVVV	number of expected GLink words per input sequence
BPIR_OutWordCountL BPIR_OutWordCountH	R/W	12 13	VVVV	number of words per output frame
BPIR_ReorderLUT	R/W	14	VVVV	Data to/from channel reorder lookup table. The address is incremented after each access and reset by the L bit in BPIR_Control. See Verilog code for LUT format.
BPIR_AuxControl	R/W	15	rrRR RR = ADC reformat mode: 0 = none 1 = invert MSB 2 = invert LSB's 3 = reserved	miscellaneous bits

* See notes on next page.

* Note 1: The capture raw data modes capture all data arriving on one link and forward the data to the DPU. They can be used to capture the ROD's Tx output (i.e., the ASM control stream) if a fiber is used to loop Tx output to Rx input. Capture begins at the next synchronous reset. Data are captured regardless of whether the receiver's RXDATA line is asserted. Capture stops when RUNNING is false (see TTCR_Status). The DPU's have the following buffer resources (assuming 40 MW/s data rate and 100 kHz trigger rate):

memory type	quantity available for capture buffer	capacity (time)	capacity (triggers)
on-chip data RAM	(50% of 128 kW) 64 kW	1.6 ms	160
off-chip SDRAM	2 MW	52 ms	5200

Captured data words have the following format:

CH	CL	see Data DPRAM capture mode section on next page
RVSEMMMMMMMM	TKrDLLLLLLLLL	24-bit format transmitted to DPU's
0000RVSEMMMMMMMM	0000TKrDLLLLLLLLL	32-bit format in the DPU's input buffer
0000RVSE0000TKrD	MMMMMMMMLLLLLLLL	32-bit format in the DPU's SDRAM

```

// TL_ (below) = value after pipelining in TTC latency pipeline
// R = TL_SYNC_RESET      from TTC FPGA      // synchronous reset
// V = TL_EXPECTED_RXDATA from TTC FPGA      // expected state of RX's RXDATA line
// S = TL_SERIAL          from TTC FPGA      // serial stream
// E = RXERROR            from GLink
// M = RX MS byte         from GLink
// T = TL_TRIGGER         from TTC FPGA
// K = LOCKED             from TTC FPGA      // AND of NP_LOCKED and TL_LOCKED
// D = RXDATA             from GLink
// L = RX LS byte         from GLink

```

Data DPRAM

DPRAM contents are identical for both Data DPRAM's.

Data DPRAM memory map:

input side address: 0Paaaaaa P = page, a = address of 48-bit word

output side address: 0P11111111 P = page, l = address of 12-bit word from lookup table

Input addresses translate to output addresses according to: output address = (input_address)*4 + dozyn, where dozyn is 3 to 0, corresponding with the twelve-bit numbers listed left to right in the tables below.

Normal mode, all 192 channels written to Data DPRAM (BPIR_InWordCount= 72*):

input address	DPRAM contents	ch	SCA	link	Description
0	N3 N2 N1 N0	0	0	0	four 12-bit samples from deserializers
1	N3 N2 N1 N0	0	0	1	
2	N3 N2 N1 N0	0	1	0	
3	N3 N2 N1 N0	0	1	1	
4	N3 N2 N1 N0	1	0	0	
5	N3 N2 N1 N0	1	0	1	
6	N3 N2 N1 N0	1	1	0	
7	N3 N2 N1 N0	1	1	1	
...	
44	N3 N2 N1 N0	11	0	0	
45	N3 N2 N1 N0	11	0	1	
46	N3 N2 N1 N0	11	1	0	
47	N3 N2 N1 N0	11	1	1	
48-55	X X X X				unused locations
56-63	SH SL X X				two 12-bit slice status registers plus two 12-bit undefined

N0's arrive on GLink LS nybble, N3's arrive on GLink MS nybble.

Capture mode, BPIR_InWordCount = 48*:

input address	DPRAM contents	Description
0	CH01 CL01 CH00 CL00	two 24-bit captured GLink values (see CH/CL format on previous page)
1	CH03 CL03 CH02 CL02	
...	...	
47	CH95 CL95 CH94 CL94	
56-63	SH SL X X	two 12-bit slice status registers plus two 12-bit undefined

*The number of valid Data DPRAM locations is dependent on the value in the BPIR_InWordCount register:

In normal mode, BPIR_InWordCount is the number of active GLink cycles (EXPECTED_RXDATA asserted) per time slice (input frame). Three validated GLink cycles yield eight N's (four per GLink receiver). Example: 72 validated GLink cycles → 192 ADC samples → input addresses 0-47 are used for samples.

In capture mode, BPIR_InWordCount is one half of the number of GLink cycles (regardless of EXPECTED_RXDATA) per time slice (input frame). Two GLink cycles yield two captured GLink values, which are written to a single DPRAM location. Example: 96 GLink cycles → input addresses 0-47 are used for 96 captured GLink values.

Slice Status Registers

Slice status registers written to Data DPRAM and optionally sent in each frame to DPU:

input address	SH	SL	Comment
56	0xfae	0xfed	constants, e.g., trailer (fae) and leader (fed)
57	RXERROR count for link 1	RXERROR count for link 0	saturating counter, cleared by sync_reset, incremented on each RXERROR (except when not LOCKED)
58	RXDATA count for link 1	RXDATA count for link 0	saturating counter, cleared by sync_reset, incremented when RXDATA does not match EXPECTED RXDATA (except when not LOCKED)
59	rPLCHHHHHHHH for link 1	rPLCHHHHHHHH for link 0	auto-alignment status -- P = phase of lock, L = phase locked, C = cycle locked, H = phase history
60	xxxxxxxxxxxxxx	xxxxxxxxxxxxxx	reserved
61*	CCCCAAAAAAAA	IIIIrrrrrrTPF	slice info from SCAC (see below or sit_bpi_common.v) IIII is the BPI FPGA chip identifier.
62*	event counter	slice counter	counters (both counters are zero for first slice of each run)
63*	rrrDEYrrrdey	rrrrrrrrLRCRS	error summary for slice, written after last data word written (see SS_ERROR_SUMMARY, below)

In normal mode each status register will be written once.

In capture mode status registers will typically be written several times (one SH/SL pair every other clock cycle).

* = In normal mode, these registers are written only when their contents are stable, e.g., after the slice's last data word is written.

In normal mode, registers not marked with * are written as soon as possible.

In capture mode, registers are written as soon as possible. The write order is 56, 57, ..., 63, 56, ...

r bits are 0.

slice info: CCCCCAAAAAAAA IIIIrrrrrrTPF

C = SCAC fault code

A = SCA read address

I = BPI FPGA chip identifier (no relation to SCAC)

T = trigger type (hi or lo priority)

P = positive/negative trigger phase

F = first time slice of trigger

SS_ERROR_SUMMARY –final error codes reported for each slice (cleared at the start of each slice):

rrrDEY rrrdey rrrrrr rrLRCRS

D	FERR_RXDATA1	RXDATA1 did not match EXPECTED_RXDATA
E	FERR_RXERROR1	RXERROR1 was asserted during at least one word of the slice
Y	FERR_RXREADY1	RXREADY1 was not asserted during at least one word of the slice
d	FERR_RXDATA0	RXDATA0 did not match EXPECTED_RXDATA
e	FERR_RXERROR0	RXERROR0 was asserted during at least one word of the slice
y	FERR_RXREADY0	RXREADY0 was not asserted during at least one word of the slice
L	FERR_LOST_LOCK	the TTC FPGA deasserted LOCKED at some time during the slice
C	FERR_CMD_MIDSLICE	the TTC FPGA sent a new TSC (command) before all data for slice had been received → data reception is aborted immediately and invalid data may be forwarded to the DPU
R	FERR_CMD_RECOVER	the TTC FPGA sent a new TSC (command) during a recovery state
S	summary	OR of all of the above

Trigger Information Stream Format

SIT Trigger Information Stream Format:

tisNop	00000000 SSSSSSSr rrrrrrrr rrrrrrrr	S = TTC FPGA status bits
tisTrigger	1rDDDDDD SSSSSST rrrrtttt tttttttt 0010LLLL LLLLLLLL LLLLLLLL LLLLLLLL 0100tttt tttttttt tttttttt tttttttt	D = TDC value, S = TTC FPGA status bits, T = trigger type, t = timestamp LSB's L = L1ID t = timestamp MSB's

ATLAS Trigger Information Stream Format:

tisNop	00000000 00000000 00000000 00000000	
tisTrigger	1rrrrrrr TTTTTTTT rrrrBBBB BBBB BBBB LLLLLLLL LLLLLLLL LLLLLLLL LLLLLLLL tttttttt tttttttt tttttttt tttttttt	T = trigger type, B = BCID L = L1ID t = timestamp (entire word is optional)

For SIT, trigger type is:

- 1 – high-priority trigger (from front panel, software, or TIM (e.g., at beamtest))
- 0 – low-priority trigger (from synchronous trigger generator)

If two triggers of different type arrive simultaneously, the trigger is assigned type 1.

For SIT, TTC FPGA status bits (MS to LS) are:

FAULT_SCAC_WRITE_ADDR	SCAC detected an illegal write address at the output of the Write Address Generator (before the gray LUT)
FAULT_SCAC_FREE_FIFO	SCAC FREE FIFO went empty
FAULT_READOUT_SEQ	readout sequencer fault (specific to LUT version of readout sequencer)
FAULT_BPIS_DAV FAULT_BPIS_START	summary of BPI supervisor faults
TMP_N	transition module not present
RUNNING	true when in a run, i.e., when not SYNC_RESET and MAX_TRIGGERS have not arrived (if STOP_AT_MAX_TRIGGERS)
LOCKED	all enabled data links are locked

Connections between TTC FPGA and BPI FPGA's

The TTC FPGA (ICU7) outputs six signals to, and receives two signals from, each of the four non-central BPI FPGA's. Each BPI FPGA receives the same output values from the TTC FPGA, though they are carried on separate point-to-point lines.

BPI FPGA Generic Name	BPI FPGA Pin	BPI FPGA Name	Description
<i>Outputs from TTC FPGA: Inputs to BPI FPGA's</i>			
P_AUXI<0>	P81	TMODE[0]	TTC mode – see table below
P_AUXI<1>	P82	TMODE[1]	
P_AUXI<2>	P83	LOCKED	1 → all enabled GLink's are locked
P_AUXI<3>	P86	EXPECTED_RXDATA	1 → RXDATA is expected to be active
P_AUXI<4>	P87	SERIAL	serial command stream – see table below
P_AUXI<5>	P88	not used	
<i>Inputs to TTC FPGA: Outputs from BPI FPGA's</i>			
P_AUXO<6>	P89	RXREADY0	lock indicators from GLink Rx's
P_AUXO<7>	P90	RXREADY1	

TMODE values:

```

tmodeSyncReset    2'b11 // synchronous reset
tmodeStopped      2'b10 // stopped
tmodeTrigger      2'b01 // running and trigger arrives
tmodeRunning      2'b00 // running
    
```

TTC serial commands

command	value	parameter bits	arrival time
tscSliceStart	4'b1001	24-bit slice info	in Normal mode, before each slice—the first four bits are guaranteed to arrive before the first EXPECTED_RXDATA of a slice
tscRunEnd	4'b1010	none	in any mode, returns input sequencer to ismDisabled
tscAlignFine	4'b1100	none	in Disabled mode, before run
tscAlignCoarse	4'b1101	none	in Disabled mode, before run
tscCheckCoarse	4'b1110	none	in Normal mode, between slices

Serial parameter bits, if any, immediately follow the four command bits.

Slice info: CCCCAAAAAAAAAA rrrrrrrrrTPF

```

C = SCAC fault code
A = SCA read address
T = trigger type (hi or lo priority)
P = positive/negative trigger phase
F = first time slice of trigger
    
```

GLink TX to ASM II (SCA Control Stream)

TX Bit	ASM II Signal	Verilog Signal	Description
15	CLK_20M	CLK_20M	optional 20 MHz write clock
14	ADCCLK	TX_RO[6]	ADC clock
13	TRIG_DATA	TX_RO[5]	connected on ASMII to DAV_N on Tx's
12	WA0	TX_WA[0]	write address
11	WA1	TX_WA[1]	
10	WA2	TX_WA[2]	
9	WA3	TX_WA[3]	
8	WA4	TX_WA[4]	
7	WA5	TX_WA[5]	
6	WA6	TX_WA[6]	
5	WA7	TX_WA[7]	
4	G[0]	TX_RO[4]	gain
3	G[1]	TX_RO[3]	
2	RD	TX_RO[2]	read pulse
1	SD	TX_RO[1]	serial read address
0	RDCLK	TX_RO[0]	read clock

TX_RO are generated by the readout sequencer.

CAL Output to TTM

The CAL output is active high for one clock cycle (25ns).

CAL is driven directly from an FPGA on the ROD and is suitable for driving an unterminated ribbon cable into a high impedance input. The CAL output is not intended to drive a 50 ohm terminator. Some ringing should be expected—the receiver threshold should be set appropriately.

The CAL signal is available at pin 15 of the BKH3 header (labeled VarL) on the TTM. All even pins on this header are connected to ground.

For CAL enables, see the TTCR_TTCC_Setup register.

CAL enables are independent of trigger enables.

CAL is not subject to the Trigger Delay Pipeline.