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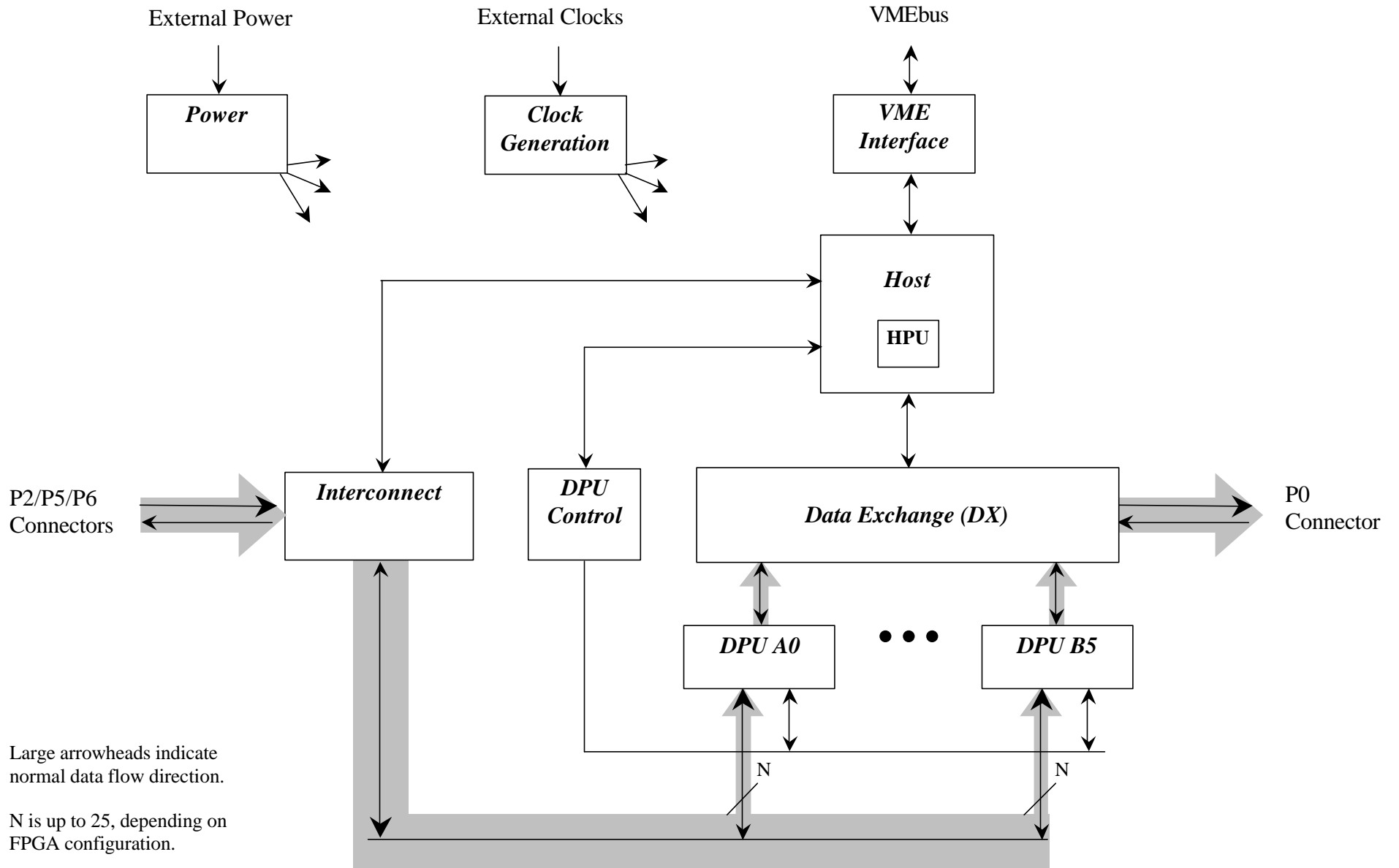
Subsystem names are in italics.  
Chip counts appear in the lower right corner of some blocks.  
Many signals are omitted for clarity.

## DSP Module Acronyms

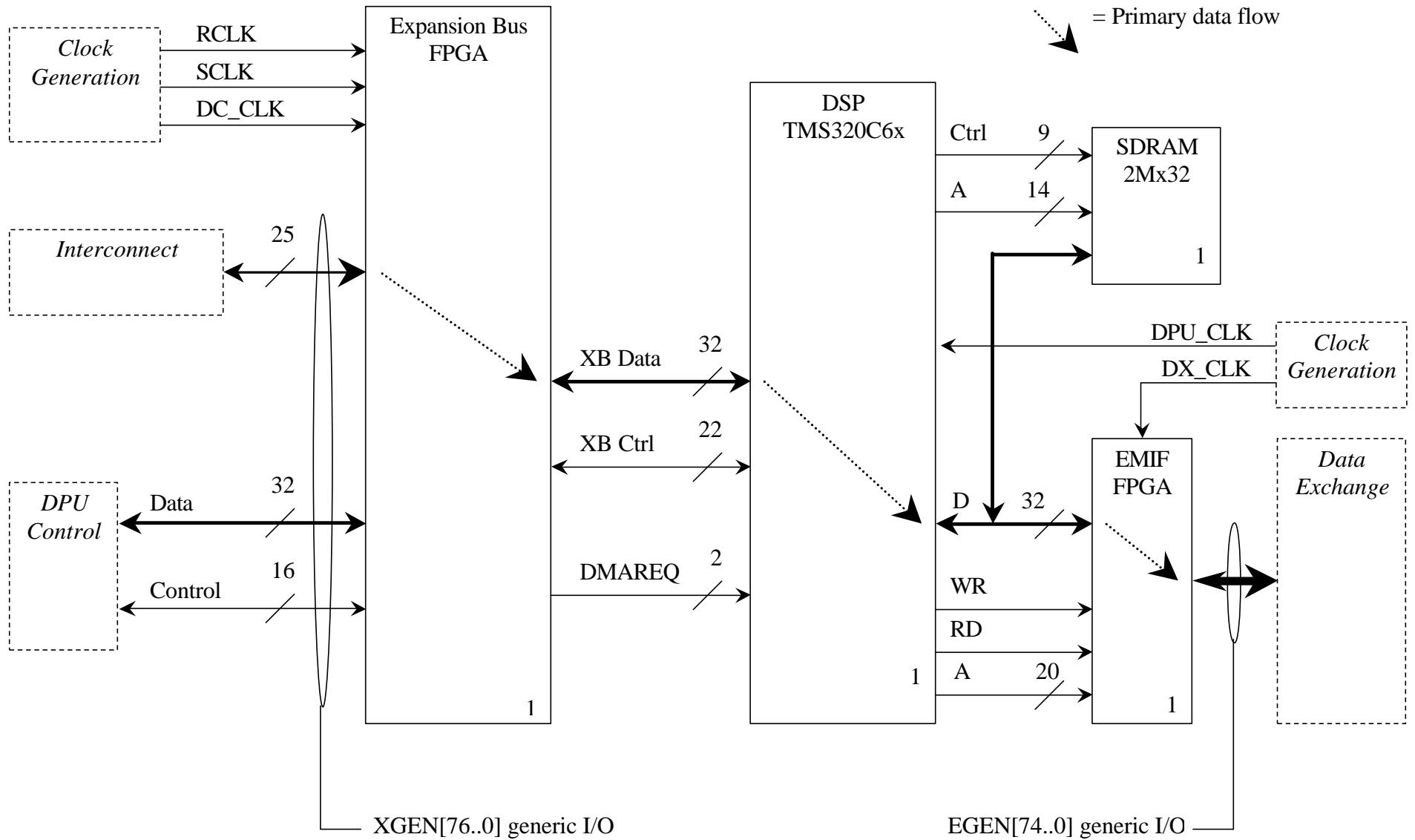
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GPU	Generic Processing Unit
HPU	Host Processing Unit
DPU	Data Processing Unit
SPU	Sparsifier Processing Unit
RPU	ROD Processing Unit

# IROD Subsystems

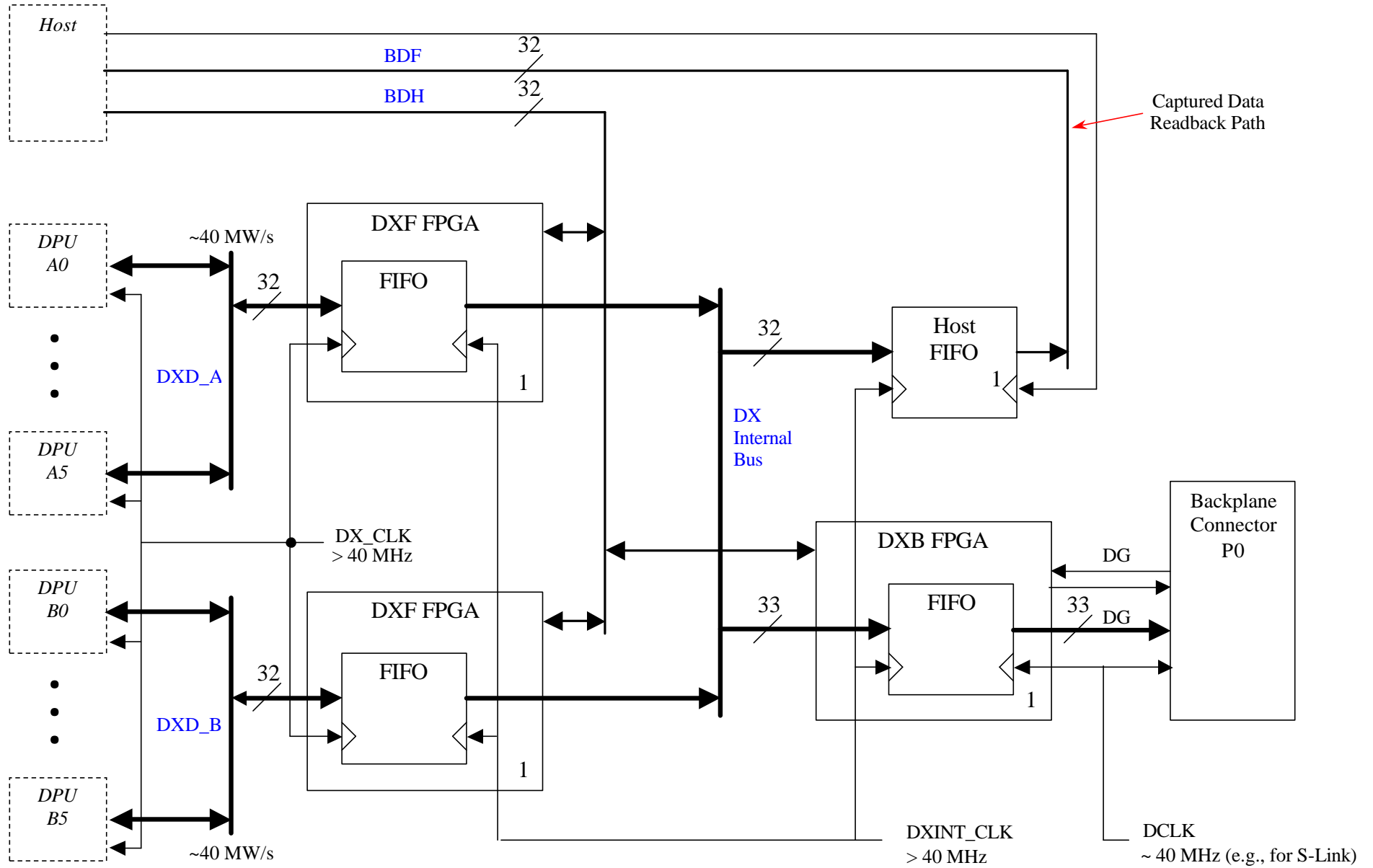


# DPU (= DSP Module = GPU = HPU)

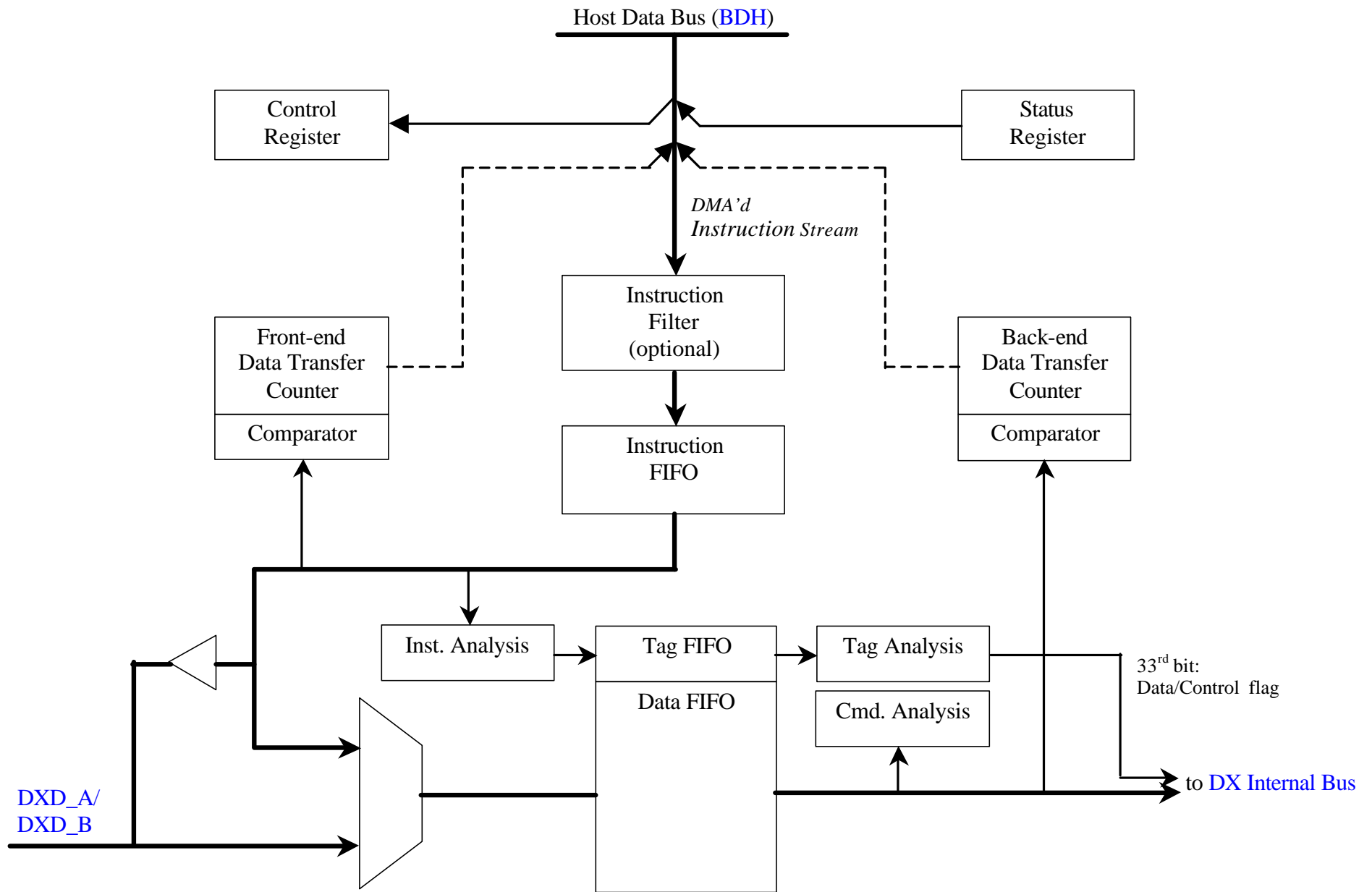


Connections and dataflow are shown for a typical DPU application.

# Data Exchange (DX)



## Data Exchange (Continued): DXF FPGA



## *Data Exchange (Continued): Instruction and Command Summary*

DX Instruction Format (HPU to DXF FPGA's) :

<b>Instruction</b>		
0000	0000 AB00 0000 0000 0000 0000 0000	NULL instruction (queued in instruction queue)
1CFF	0001 AB00 EDSd 00dd dddd 00ss ssss	run front sequence
1CFF	0010 AB00 EDS0 00dd dddd NNNN NNNN	write N data words to destination
1CFF	0010 AB00 0001 0000 0000 NNNN NNNN	write N data words to data FIFO
0000	0011 AB00 0000 0000 0000 NNNN NNNN	write N command words to data FIFO
0000	0100 AB00 0000 0000 0000 0000 0000	notify front (send pulse to HPU)
0000	0101 AB00 0000 0000 0000 0000 0000	reset front counter
0000	0110 AB00 0000 0000 0000 0000 0000	capture front counter
0000	0111 AB00 0000 VVVV VVVV VVVV VVVV	verify front counter LSB's equal V

Tag + Data Format (input to DXF FPGA's Data+Tag FIFO):

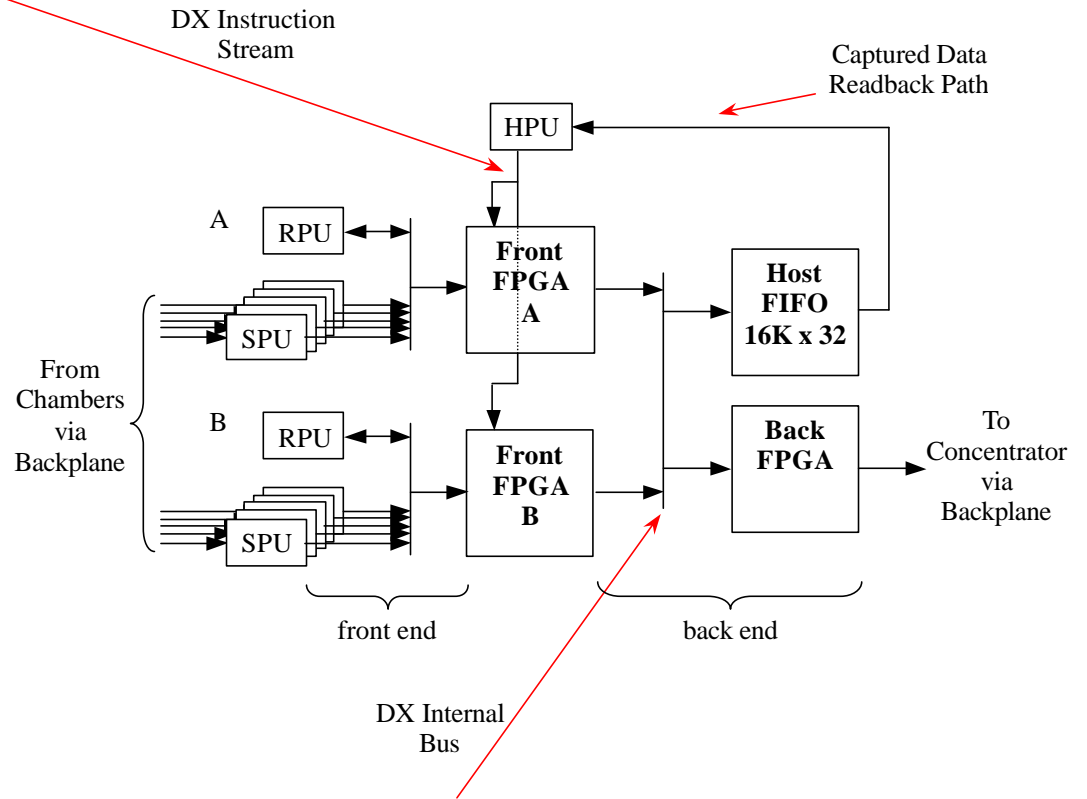
<b>Data queued in the data FIFO:</b>		queued via write N data words instruction
Tag	Data	
1CFF	-- data --	data
1000	xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx	(no effect, but counted by data counter)

<b>DX Commands queued in the data FIFO:</b>		queued via write N command words instruction
Tag	Data	
0000	0000 0000 0000 0000 0000 0000 0000 0000	NOP
0000	0011 0000 0000 0000 0000 0000 0000 0000	release output bus to other DXF FPGA
0000	0100 0000 0000 0000 0000 0000 0000 0000	notify back (send pulse to HPU)
0000	0101 0000 0000 0000 0000 0000 0000 0000	reset back counter
0000	0110 0000 0000 0000 0000 0000 0000 0000	capture back counter
0000	0111 0000 0000 0000 VVVV VVVV VVVV VVVV	verify that back counter LSB's equal V

- A, B = target of instruction (DX half A, DX half B, or both)
- E = end of event flag (optional)
- F = destination FIFO enables (ROL FIFO, Host FIFO, both, or neither)
- C = control bit, sent along with data to back end—typically used with S-Link to mark event start and end
- s = source target(s)
- d = destination target(s) (the leftmost d for “run front sequence” represents the DXF FPGA's internal data FIFO)
- D = DMA channel for destination (e.g., one channel for event data, one for bulk data)
- S = DMA channel for source (e.g., one channel for event data, one for bulk data)
- N = count of data/command words that immediately follow the current instruction
- V = value to compare against back/front counter LSB's

## Data Exchange (Continued): ATLAS CSC Example Application

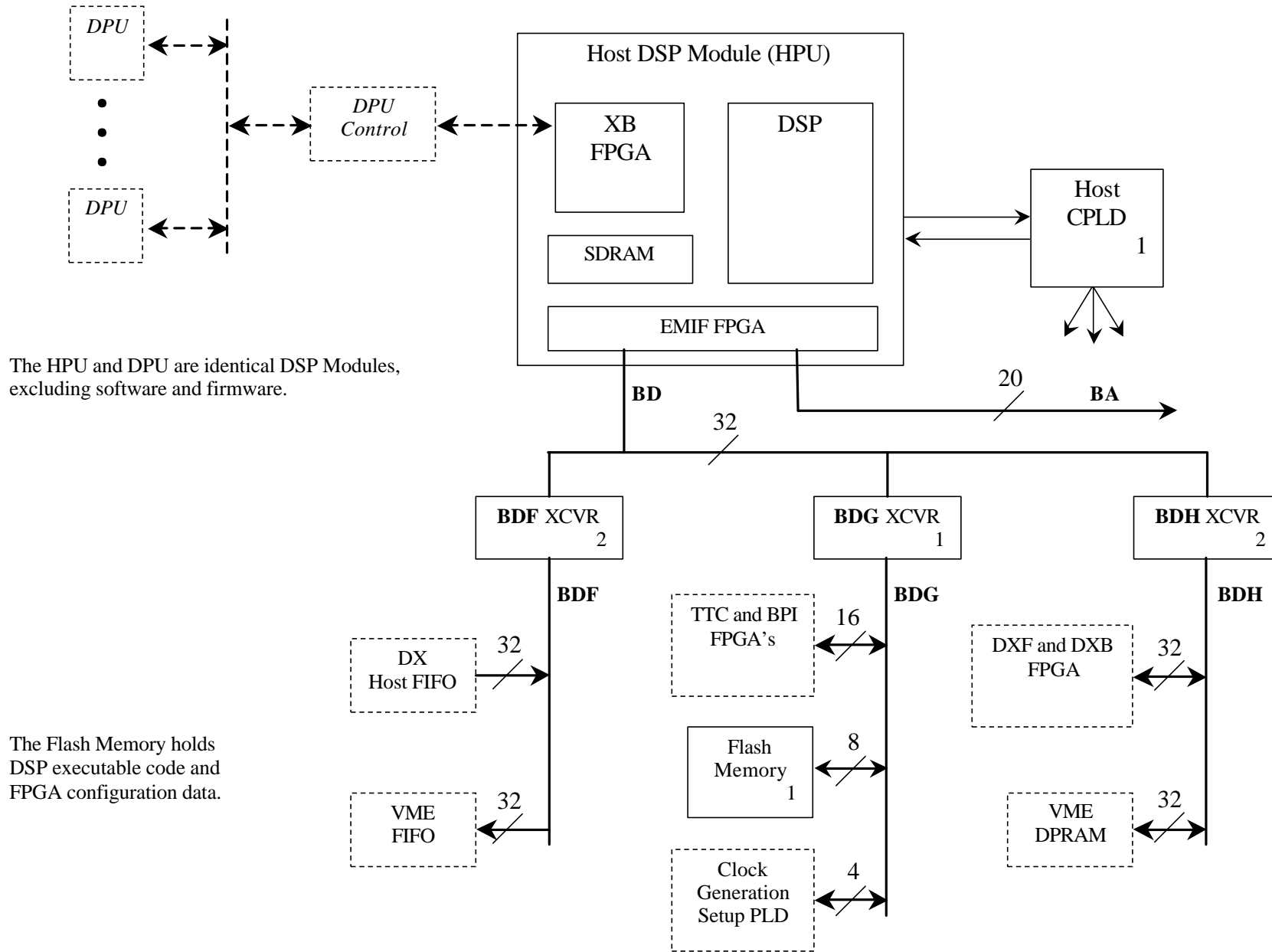
Side	DX Instruction Stream	Word Count
	<i>Build Sparsified Event: SPU's ® RPU</i>	
A and B	run front sequence: SPU's → RPU source: SPU0, SPU1, SPU2, SPU3, SPU4 destination: RPU	1
	<i>Build Final Event: RPU's ® Back End</i>	
A	write leader to back end: CSC ROD leader	1 +2
A and B	run front sequence: RPU's → back end source: RPU destination: back end	1
A	write command word to back end: release DX Internal Bus (release it to B)	1 +1
B	write trailer: CSC ROD trailer	1 +2
B	write command word to back end: Release DX Internal Bus (return it to A)	1 +1
	<b>total</b>	<b>12 words/L1</b>
	<b>typical HPU DMA rate to DX</b>	<b>1.2 MW/s</b>



Typical values are based on  
 L1 rate = 100 kHz,  
 acceptance window = 25 ns,  
 and these conservative assumptions:  
 no neutron rejection,  
 flux = 1500 Hz/cm<sup>2</sup>,  
 five channels are read out per hit.

Driver	DX Internal Bus Stream	Word Count
A	CSC ROD leader	2
A	data from RPU A (1 chamber)	10 typ
B	data from RPU B (1 chamber)	10 typ
B	CSC ROD trailer	2
	<b>typical total</b>	<b>24 words/L1</b>
	<b>typical rate to Concentrator</b>	<b>2.4 MW/s</b>

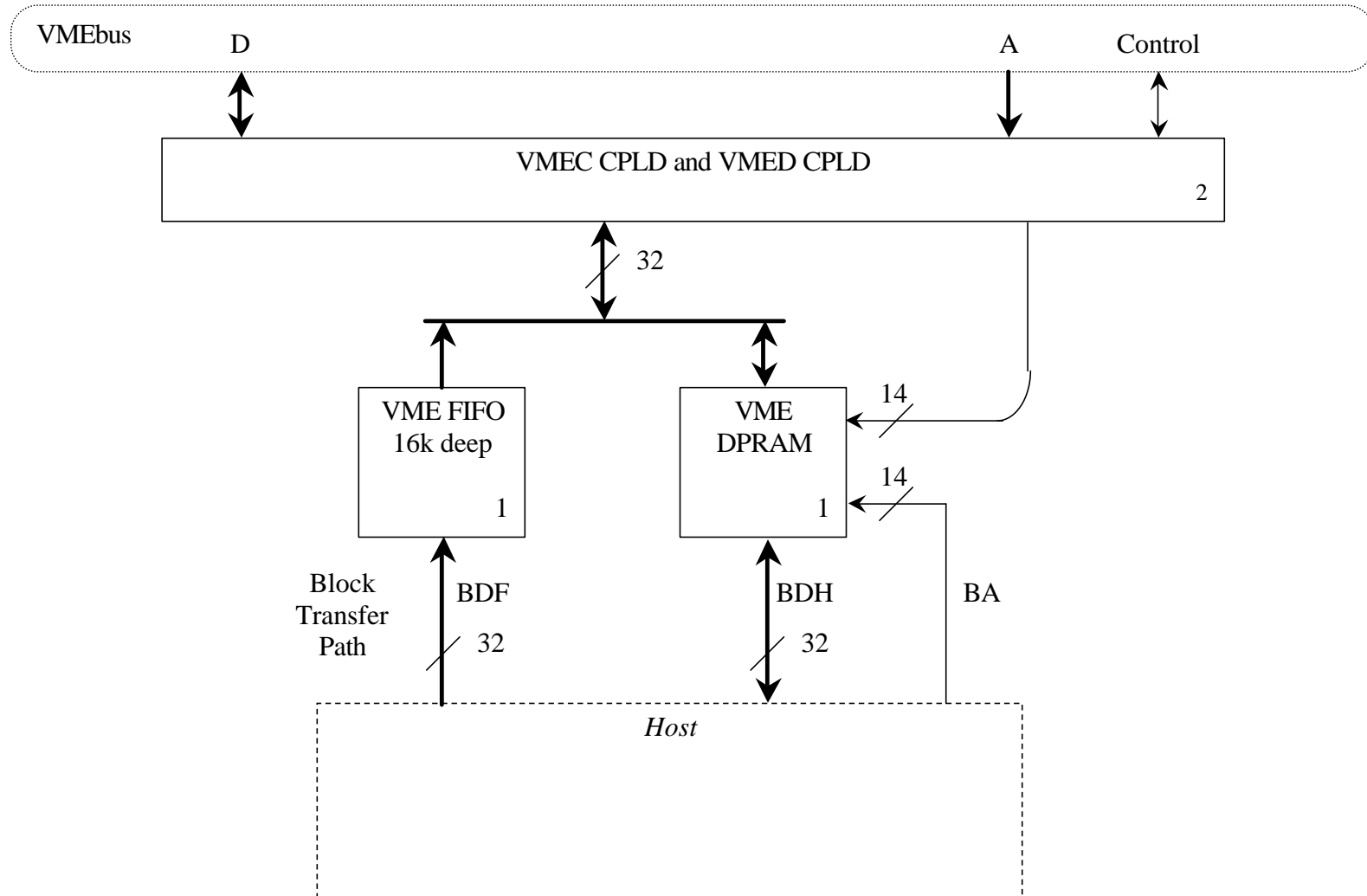
# Host



The HPU and DPU are identical DSP Modules, excluding software and firmware.

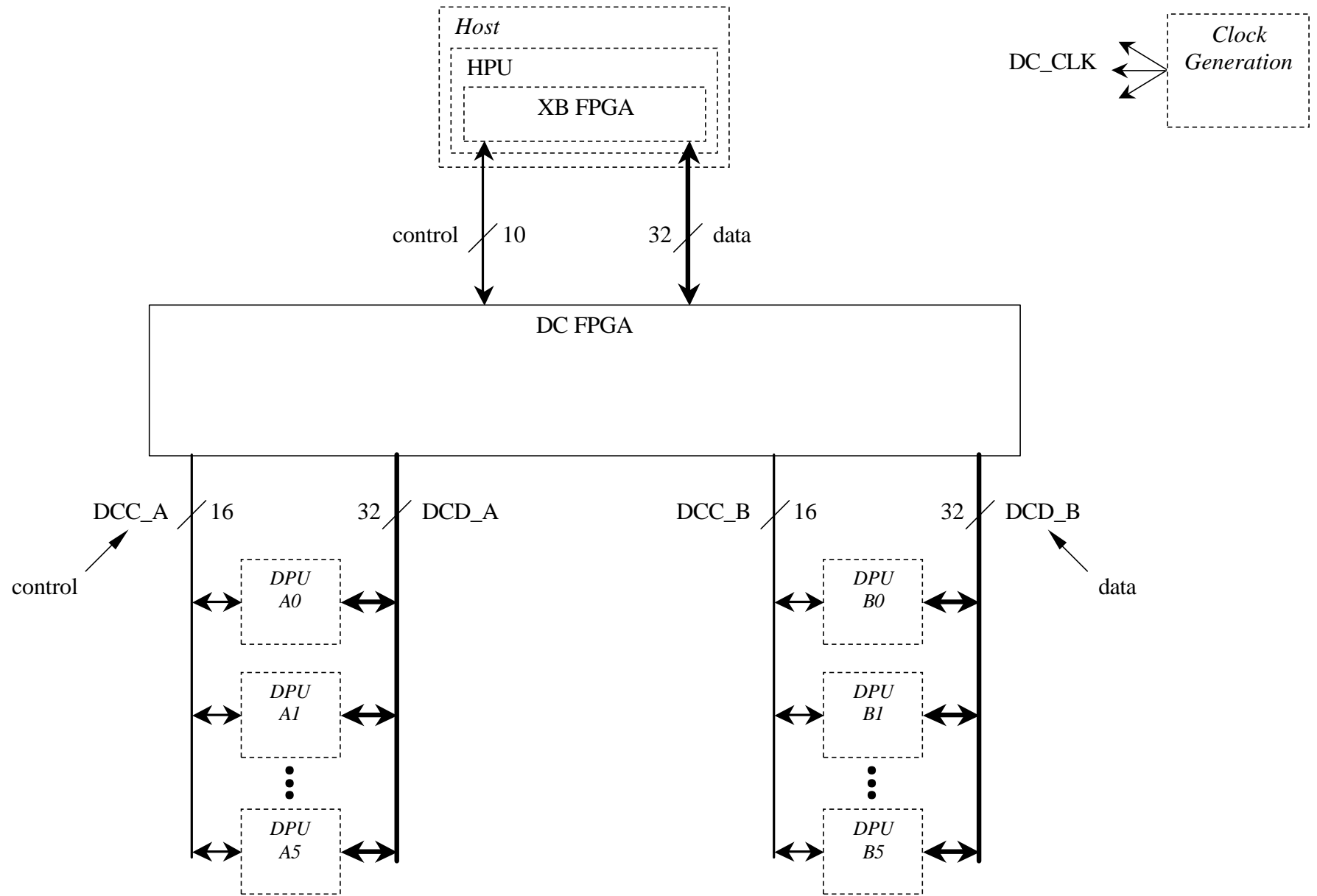
The Flash Memory holds DSP executable code and FPGA configuration data.

# VME Interface

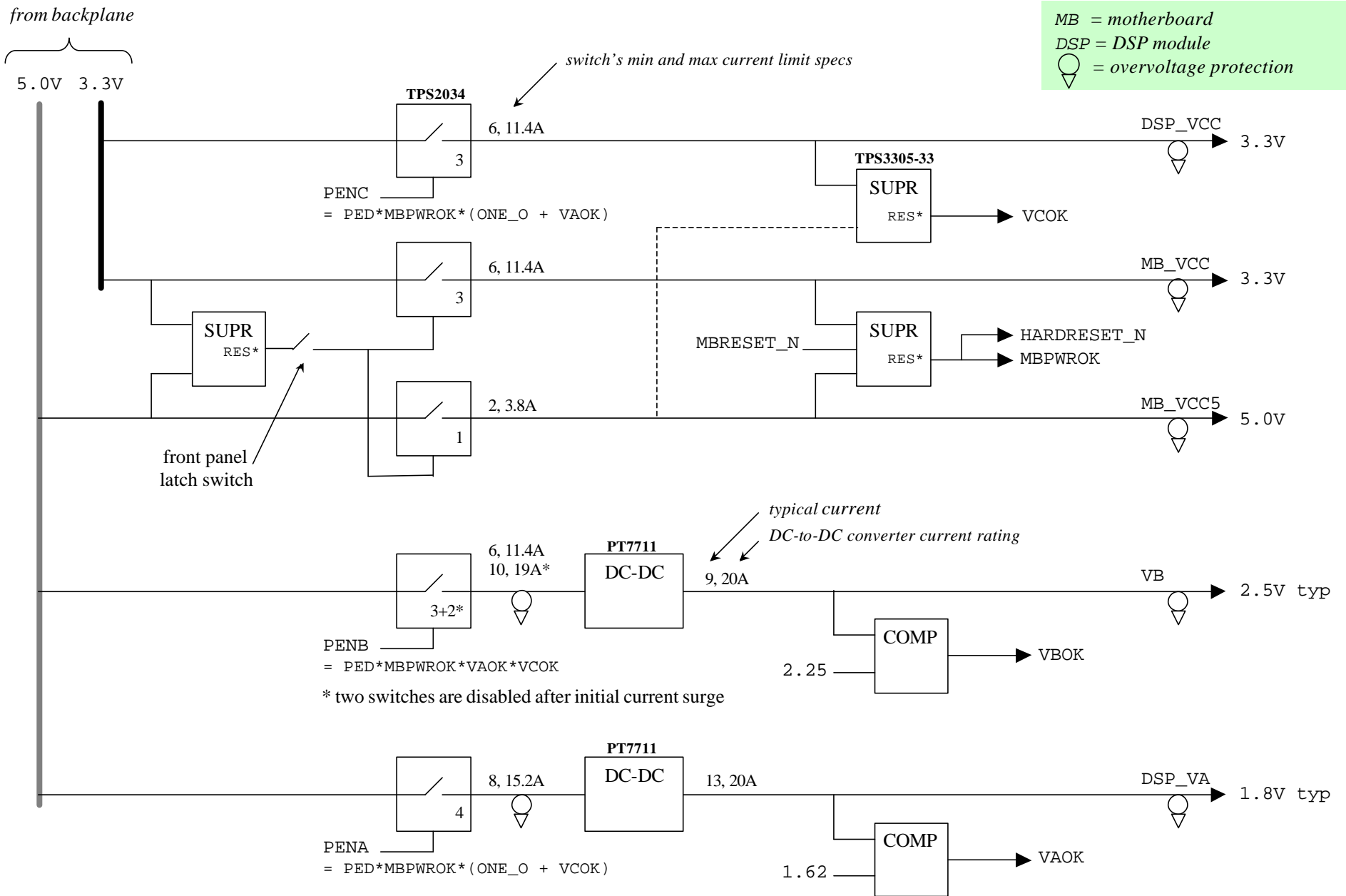


Not Shown:  
 Buffers  
 optional CS/CSR flash memory

# DPU Control (DC)

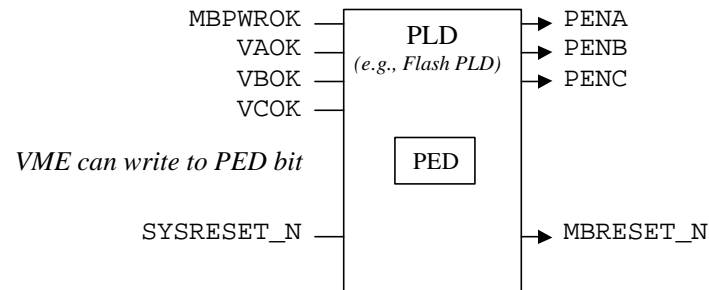


# Power



## Power (Continued)

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All switch enables are active high and have a 1k pulldown.  
A Schottky diode across each switch protects it from a sudden loss of input voltage.  
ONE\_O is a one-second one-shot signal internal to the PLD. It is triggered by the setting of PED.

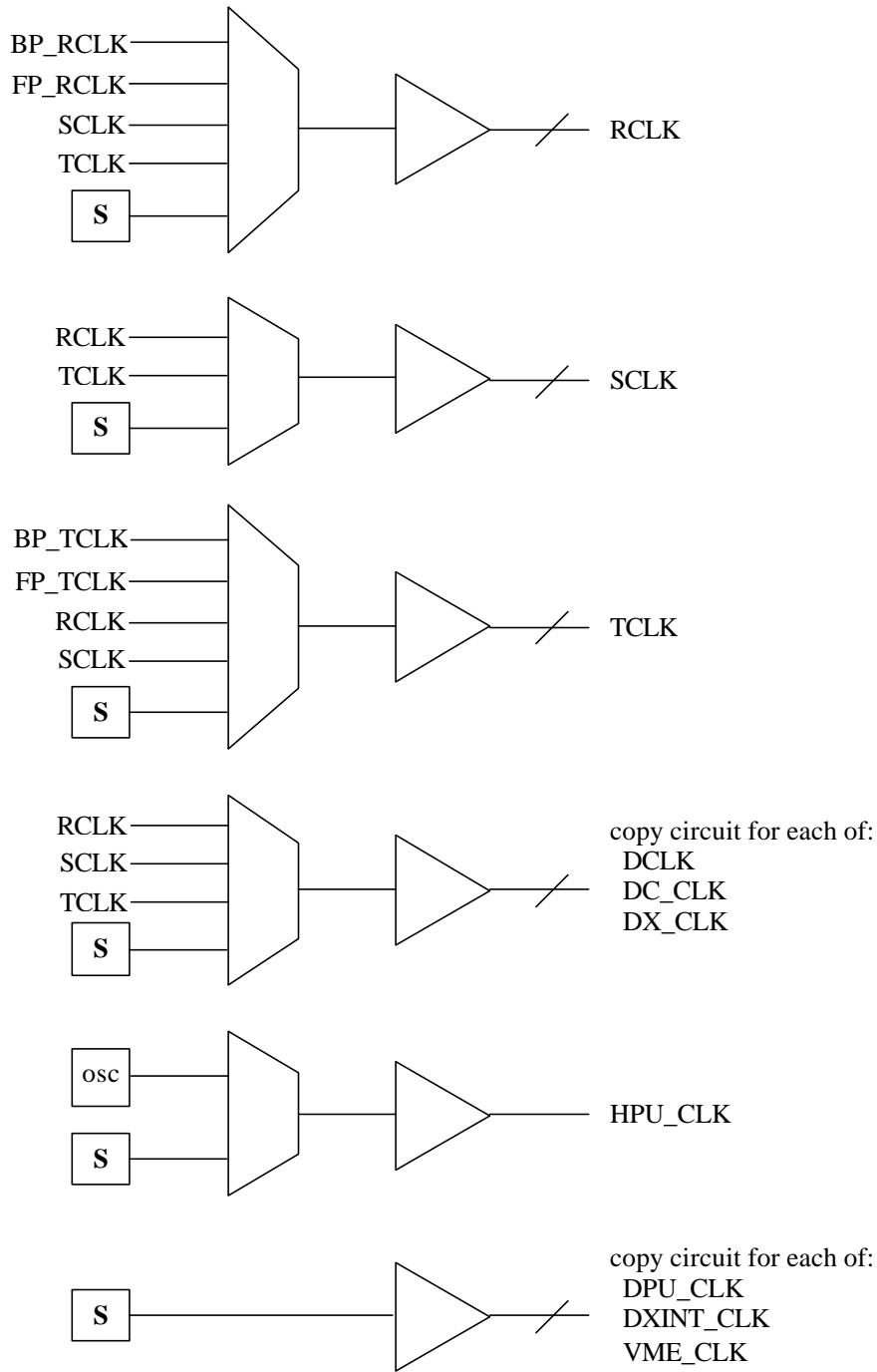
### Power Subsystem Goals:

- protect ROD from overvoltage on each power supply
- protect ROD from negative voltage on each power supply
- protect DSP's from failed VCC or VCORE
- limit ROD current
- allow RCC to orchestrate a slow start of the ROD
- allow RCC to perform a hard reset of the ROD
- sequence supplies properly:
  - satisfy DSP's powerup requirements
  - power up motherboard MB\_VCC and MB\_VCC5 only if both backplane supplies, B\_VCC and B\_VCC5 are valid
  - supply initial 500 mA each Spartan II FPGA's (18.5A total)
- monitor supply currents



## Clock Generation (Simplified)

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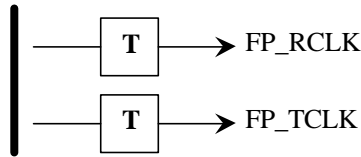


osc = crystal oscillator

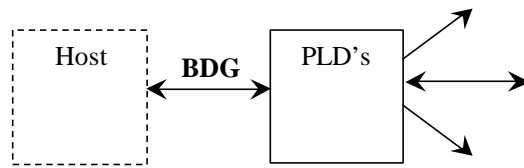
S = frequency synthesizer

## Clock Generation (Continued)

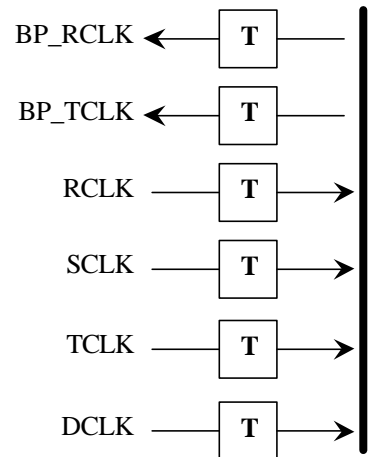
Front Panel



*setup signals to mux's,  
synthesizers, etc.*



Backplane



*BP = backplane, FP = front panel.*

Component summary:

Chip	descr.	N	mA ea	mA total	\$each	\$total
CDC2516	pll buffer	5	150	750	\$4	\$20
CDC2510	pll buffer	5	100	500	3	15
CDC319	buffer	4	30	120	3	12
PRN1102433	res. pack	4	0	0	1	4
FS6377-01	synth.	10	40	400	4	40
W170-01	pll buffer	3	20	60	3	9
CBTLV3253	mux	7	5	35	2	14
TBD	PLD	2	10	20	5	10
TBD	translator	8	10	80	2	16
TBD	oscillator	2	25	50	2	4
<b>Total</b>		<b>50</b>		<b>2015</b>		<b>\$144</b>

Clock Summary:

Name	Typical Use	typ rate, MHz
BP_RCLK	receive clock input from backplane	40-80
FP_RCLK	receive clock input from front panel	40-80
RCLK	receive clock	40-80
SCLK	copy of TTC clock, if needed by HPU and/or DPU's	40
BP_TCLK	TTC clock input from backplane	40
FP_TCLK	TTC clock input from front panel	40
TCLK	TTC clock	40
HPU_CLK	HPU DSP clock (multiplied by PLL in DSP)	50-100
DPU_CLK	DPU DSP clock (multiplied by PLL in DSP)	50-100
DXINT_CLK	Data Exchange internal clock	50-70
DCLK	Data Exchange output clock, e.g., S-LINK clock (UCLK)	40
VME_CLK	clock to VME PLD's	50
DC_CLK	DPU Control clock, also functions as DSP expansion bus clock	40
DX_CLK	Data Exchange clock	40-50