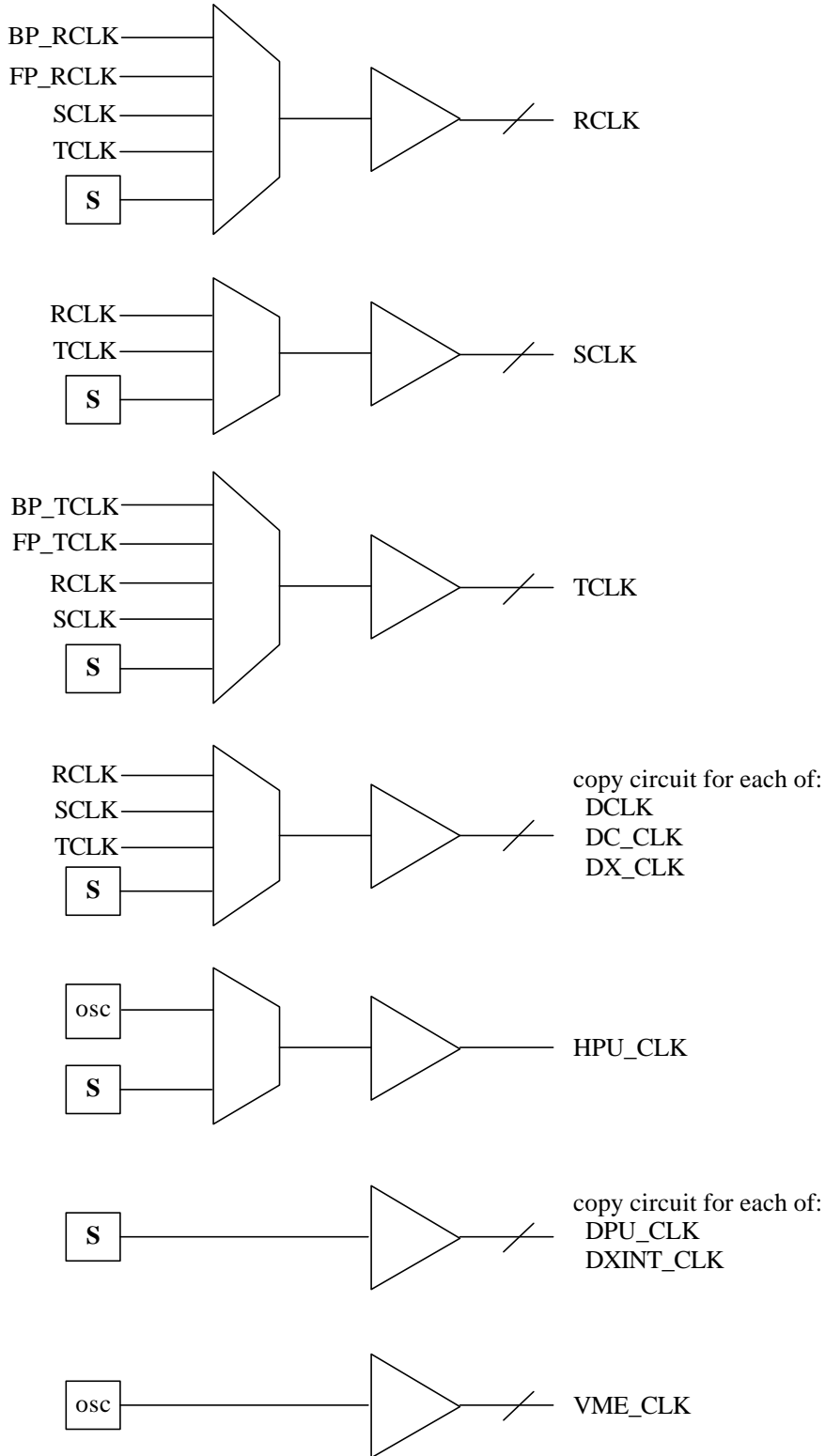


## Clock Generation (Simplified)

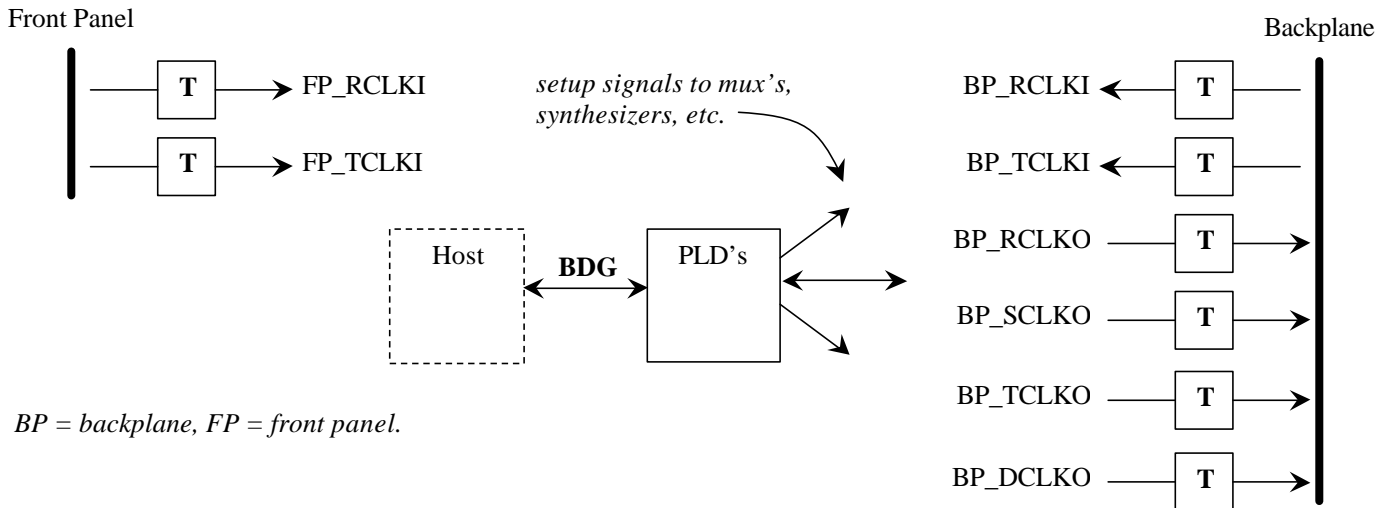
---



**S** = frequency synthesizer

**osc** = crystal oscillator

## Clock Generation (Continued)



*BP = backplane, FP = front panel.*

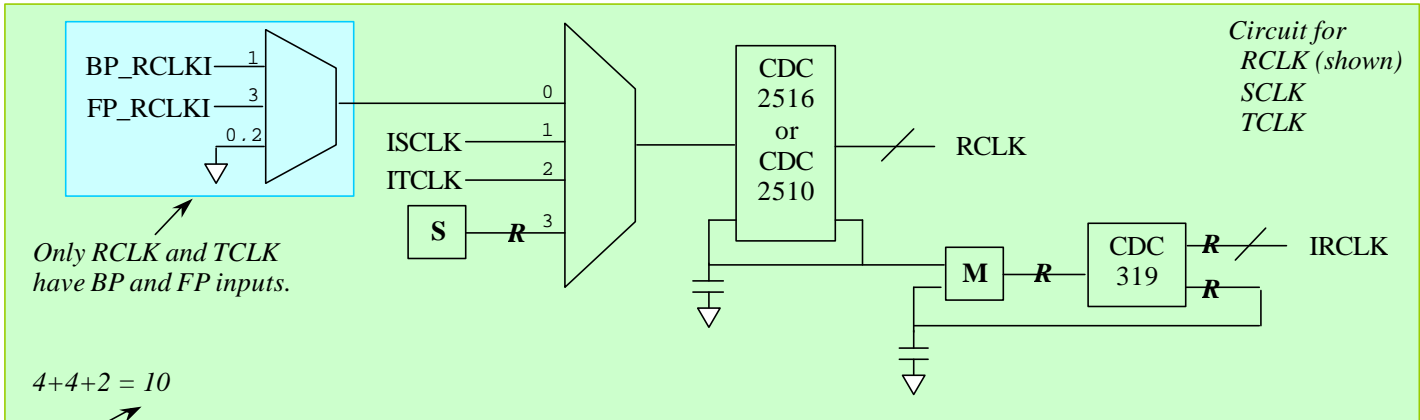
### Component summary:

Chip	descr.	N	mA ea	mA total	\$each	\$total
CDC2516	pll buffer	4	150	600	\$4	\$16
CDC2510	pll buffer	6	100	600	3	18
CDC319	buffer	4	30	120	3	12
PRN1102433	res. pack	4	0	0	1	4
FS6377-01	synth.	9	40	360	4	36
W170-01	pll buffer	3	20	60	3	9
CBTLV3253	mux	11	5	55	2	22
XC95144XL-7TQ100C	PLD	2	10	20	10	20
TBD	translator	8	10	80	2	16
TBD	oscillator	3	25	75	2	6
<b>Total</b>		<b>50</b>		<b>1970</b>		<b>\$159.00</b>

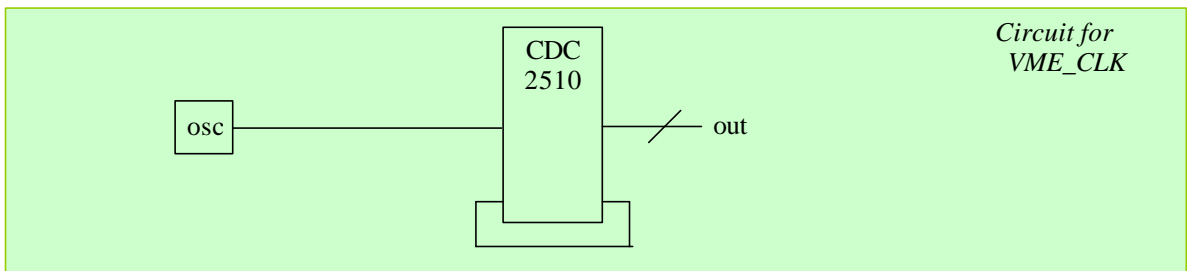
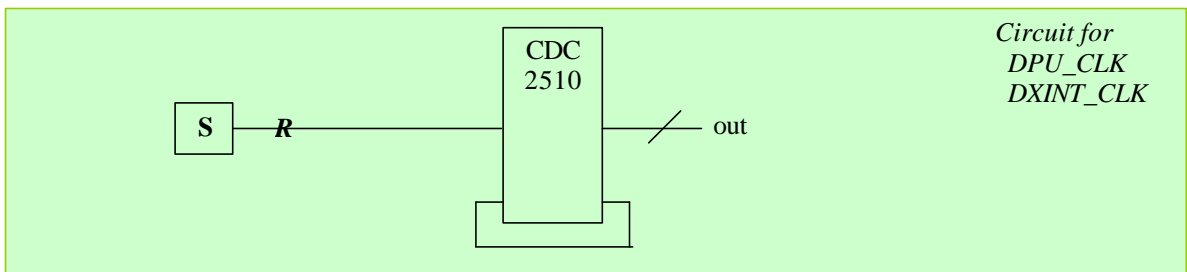
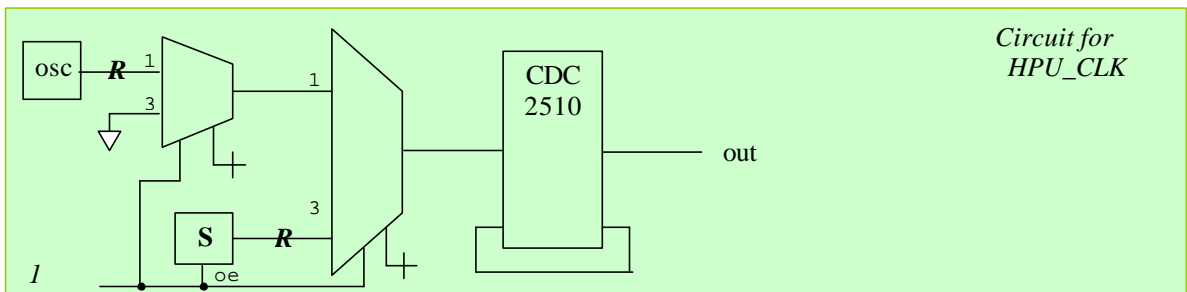
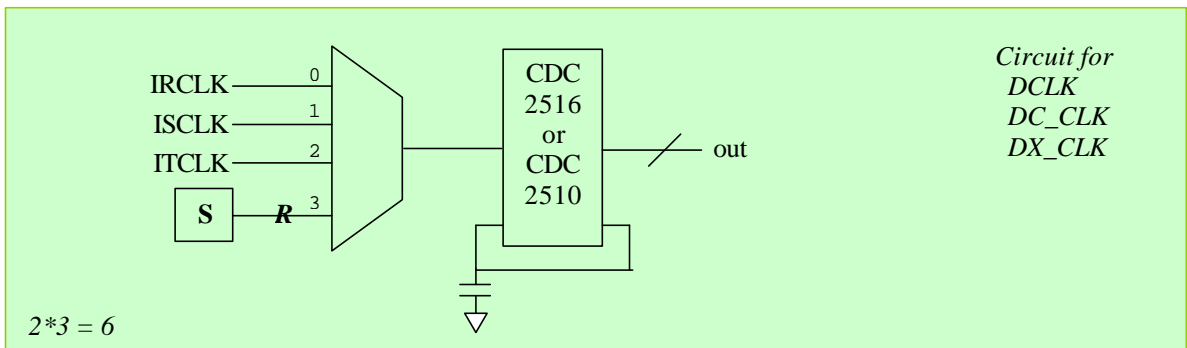
### Clock Summary:

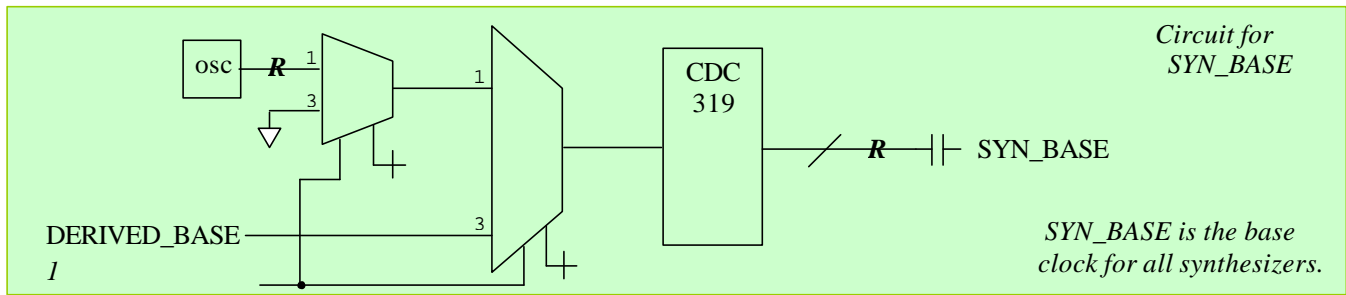
Name	Typical Use	typ rate, MHz
BP_RCLK	receive clock input from backplane	40-80
FP_RCLK	receive clock input from front panel	40-80
RCLK	receive clock	40-80
SCLK	copy of TTC clock, if needed by HPU and/or DPU's	40
BP_TCLK	TTC clock input from backplane	40
FP_TCLK	TTC clock input from front panel	40
TCLK	TTC clock	40
HPU_CLK	HPU DSP clock (multiplied by PLL in DSP)	50-100
DPU_CLK	DPU DSP clock (multiplied by PLL in DSP)	50-100
DXINT_CLK	Data Exchange internal clock	50-70
DCLK	Data Exchange output clock, e.g., S-LINK clock (UCLK)	40
VME_CLK	clock to VME PLD's	50
DC_CLK	DPU Control clock, also functions as DSP expansion bus clock	40
DX_CLK	Data Exchange clock	40-50

# Clock Generation (Details)



*Total mux  
addresses for  
all circuits*





**osc** = crystal oscillator                      **R** = 30 ohm series terminator

**S** = frequency synthesizer                      All clocks are disabled (driven low) until VCOK except:  
VME\_CLK

**M** = frequency multiplier                      BOOT\_CLK

**PLD's:**

NOISY PLD pin summary

pins	count	description
clock inputs for frequency measurement	10	
host bus	11	8 data, 1 addr, 1 STB_N, 1 WR_N
setup bus to QUIET PLD	11	8 data, 1 addr, 1 STB_N, 1 WR_N
BOOT_CLK	1	
MEAS_CLK	1	
PROG* for FPGA's	37	12*2 (DPU) + 11 (MB) + 2 (BK) minimum
<b>Total</b>	<b>72</b>	
Total I/O pins for XC95144XL in TQ100	81	includes 3 GCK, 1 GSR, 4 GTS

QUIET PLD pin summary

pins	count	description
clock inputs for generating SYN_BASE	3	I_RCLK, I_SCLK, I_TCLK
DERIVED_BASE output	1	one of above clock inputs divided down
setup bus from NOISY PLD	11	8 data, 1 addr, 1 STB_N, 1 WR_N
mux addresses	20	10 + 6 + 2 + 2
multiplier factor select	6	3 circuits * 2 wire/circuit
CDC319 serial clock	4	
synthesizer serial clock	10	
synthesizer SEL_CD	1	
synthesizer PD	1	
serial data for synthesizers and CDC319's	1	
oscillator output enable	2	for HPU and SYN_BASE oscillators
<b>Total</b>	<b>60</b>	
Total I/O pins for XC95144XL in TQ100	81	includes 3 GCK, 1 GSR, 4 GTS

# Clock Generation PLD Registers

Clock Registers (Quiet PLD)	Address	Model			
		mux	synth	driver	mult
	offset → base ↓	+0	+1	+1	+2
IRCLK	20	n/a	n/a	sclk	mult
ISCLK	24	n/a	n/a	sclk	mult
ITCLK	28	n/a	n/a	sclk	mult
SYN_BASE	2C	muxB	n/a	sclk	n/a
RCLK	40	muxR	sclk	n/a	n/a
SCLK	44	muxS	sclk	n/a	n/a
TCLK	48	muxT	sclk	n/a	n/a
DCLK	4C	mux4	sclk	n/a	n/a
DC_CLK	50	mux4	sclk	n/a	n/a
DX_CLK	54	mux4	sclk	n/a	n/a
HPU_CLK	58	mux2	sclk	n/a	n/a
DPU_CLK	5C	n/a	sclk	n/a	n/a
DXINT_CLK	60	n/a	sclk	n/a	n/a
VME_CLK	none	n/a	n/a	n/a	n/a

Model	Register Layout	Register Reset Value
mult	xxxxxxxM M = 0: multiply by 1 * M = 1: multiply by 2	xxxxxxx0
sclk	xxxxxxxK K = serial clock	xxxxxxx1
mux2	xxxxxxxS S = 0: use osc * S = 1: use synth	xxxxxxx0
mux4	xxxxxxxSS SS = 0: use IRCLK SS = 1: use ISCLK SS = 2: use ITCLK SS = 3: use synth *	xxxxxxx11
muxB	xxxxxxxS S = 0: use osc * S = 1: use DERIVED_BASE	xxxxxxx0
muxR	xxxxPPSS SS = 0: use clock selected by PP SS = 1: use ISCLK SS = 2: use ITCLK SS = 3: use synth * PP = 0: GND * PP = 1: BP_RCLKI PP = 2: GND PP = 3: FP_RCLKI	xxxx0011
muxS	xxxxxxxSS SS = 0: GND SS = 1: use IRCLK SS = 2: use ITCLK SS = 3: use synth *	xxxxxxx11
muxT	xxxxPPSS SS = 0: use clock selected by PP SS = 1: use IRCLK SS = 2: use ISCLK SS = 3: use synth * PP = 0: GND * PP = 1: BP_TCLKI PP = 2: GND PP = 3: FP_TCLKI	xxxx0011

Other Registers	PLD	Address	Model	Reset Value
SD serial data shared by synthesizers and drivers	Quiet	10	xxxxxxxD D = serial data	xxxxxxx0
SEL_CD to SEL_CD pin of all synthesizers	Quiet	14	xxxxxxxS S = SEL_CD	xxxxxxx1
DERIVED_SOURCE source from which to derive DERIVED_BASE	Quiet	20	xxxxxxxSS SS = 0: source = 0 * SS = 1: source = IRCLK SS = 2: source = ISCLK SS = 3: source = ITCLK	xxxxxxx00
DERIVED_DIVIDE factor by which to divide source of DERIVED_BASE	Quiet	24	xxxxxxxDD DD = 0: out = 0 * DD = 1: out = source DD = 2: out = source/2 DD = 3: out = source/4	xxxxxxx00
MEAS_SEL clock to measure	Noisy	90	xxxxSSSS SSSS = 0: RCLK SSSS = 1: DX_CLK SSSS = 2: SCLK SSSS = 3: DC_CLK SSSS = 4: DPU_CLK SSSS = 5: TCLK SSSS = 6: DCLK SSSS = 7: HPU_CLK SSSS = 8: DXINT_CLK SSSS = 9: VME_CLK SSSS = F: <none>	xxxx1111
MEAS_START (write)	Noisy	91	xxxxxxxS S = 0 -> 1: start measurement	xxxxxxx0
MEAS_BUSY (read)	Noisy	91	xxxxxxxD D = 0: measurement done D = 1: measurement not done	xxxxxxx0
MEAS_L LS byte of frequency measurement	Noisy	92	MMMMMMMM: LS byte of measurement	00000000
MEAS_H MS byte of frequency measurement	Noisy	93	MMMMMMMM: MS byte of measurement	00000000
TEST	Noisy	94	TTTTTTTT: read/write bits	00000000
PROGRAM_BK0 PROGRAM_BK1	Noisy	C0 C1	xxxxxxxP 0 = PROGRAM_N is asserted 1 = PROGRAM_N is deasserted	xxxxxxx0
PROGRAM_DC	Noisy	C4	"	"
PROGRAM_DXFA PROGRAM_DXFB PROGRAM_DXB	Noisy	C8 C9 CA	"	"
PROGRAM_TTC	Noisy	DF	"	"
PROGRAM_IC0- PROGRAM_IC5	Noisy	D0-D5	"	"
PROGRAM_DPU	Noisy	E0 + 000FSDDD F = FPGA S = side D = DPU	"	"
LOCK security lock, details TBD	Noisy	TBD	TBD	TBD

Clock Generation Address bit:

0: write to / read from Pointer    1: write to / read from register addressed by Pointer

Clock Generation Registers:

address 0x00 – 0x7f: Quiet PLD    address 0x80 – 0xff: Noisy PLD