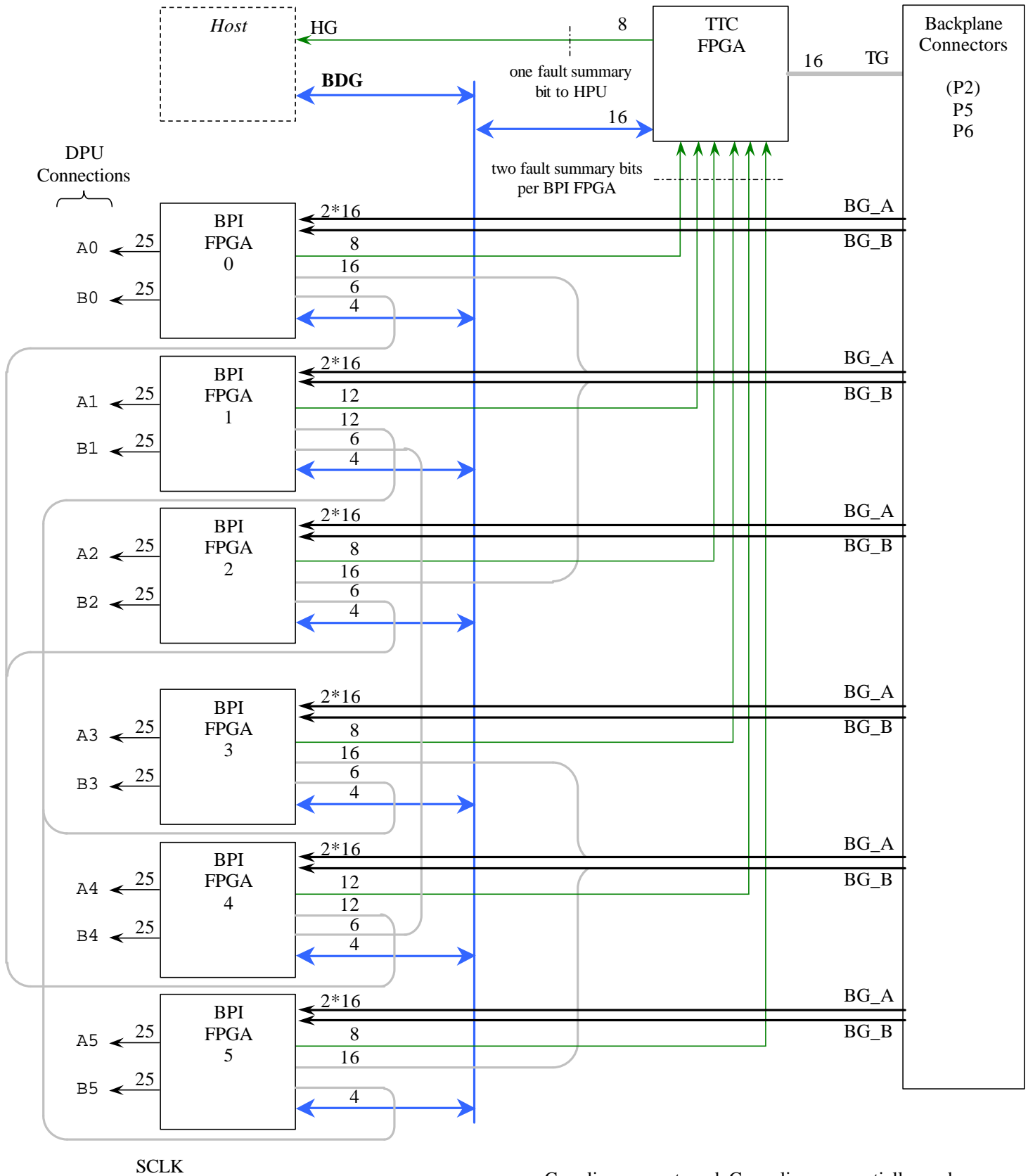


# IROD Interconnect Subsystem—CSC Application



Gray lines are not used. Green lines are partially used.  
 The BPI FPGA connected to the RPU's (e.g. #5), is not used.

## General Features

Chambers supported:	2	chambers per ROD
Data stream from CTM to BPI FPGA's:	2 16 RCLK: 80 actively aligned	streams per BPI FPGA bits/SPU MHz see Active Data Alignment section
Data stream from BPI FPGA's to SPU's:	2 1+24 SCLK: < 70 fixed alignment	streams per BPI FPGA DAV + data bits/SPU MHz

## Data Format (Except During Active Data Alignment)

Data from the CTM to the BPI FPGA's are formatted as blocks of 16-bit words. Each block contains data and status for one SPU time slice (i.e., one layer's data for one sample period). There is no DAV line. The first word of the block is the header word, with value 0x0b0b (beginning of block). The header word is followed by a fixed number of payload words. The payload words are followed immediately by one stop word, with value 0xe0b0 (end of block). Words between blocks are zero.

The block's payload consists of three-word triplets. One triplet contains four 12-bit values, one value carried on each nybble. A lookup table in the Rx FPGA determines the order of the 12-bit values. For details, see "Data Buffering Detail" in CTM\_Overview\_xx.pdf.

The header/stop logic in the ROD's BPI FPGA's checks and discards the header and stop words. Any header or stop error causes a fault. Neither the block that caused the fault nor any subsequent block is transmitted to the DPU. The fault affects only the buffer/deserializer (A or B) that experienced the fault.

Shift registers in the BPI FPGA's deserialize a block's triplets, allowing four 12-bit values to be written to DPRAM every three clock cycles (two idle cycles followed by a 48-bit write in one cycle). Once a block's entire payload is in the DPRAM, the block is sent to the DPU. The BPI FPGA writes and reads the DPRAM in sequential order. There is no reordering lookup table in the BPI FPGA.

A 25-bit bus carries data from BPI FPGA to DPU. One of the bits is DAV (data valid), so blocks consist of payload only.

## Active Data Alignment

The CTM provides RCLK to the ROD. Its frequency is 80 MHz. Its phase is arbitrary with respect to all other ROD clocks.

All BPI FPGA's receive approximately identical copies of RCLK, though the phase of each BPI FPGA's copy is irrelevant.

The CTM's Rx FPGA's can shift the phase of each 16-bit data stream under HPU control:

shift resolution:       30-50 ps  
shift range:            ~10 ns

The Rx FPGA's contain a pattern generator for each data stream. The BPI FPGA's contain a pattern verifier. Prior to reception of chamber data, the HPU must use the pattern generators and pattern verifiers to determine an error-free phase setting for each data stream.

The HPU must scan the entire phase range of each data stream and analyze the error counts recorded by the stream's pattern verifier.

The HPU should set each stream's phase to the center of the widest error-free phase range.

The pattern generator and pattern verifier support the following patterns:

<b>pattern name</b>	<b>pattern</b>	<b>verification rule</b>
otestAlternate	0x0000, 0xffff, 0x0000, 0xffff, ...	no error if $((D == 0) \text{ or } (D == -1)) \text{ and } (D_N == \sim D_{N-1})$
otestCount	0x0000, 0x0001, 0x0002, 0x0003, ...	no error if $(D_N - 1) == D_{N-1}$

The pattern output is continuous with no headers or trailers. The data deserializers and buffers in the BPI FPGA are disabled while the pattern verifier is operating.

## BPI FPGA Registers

<i>In BPI FPGA, directly accessible:</i>	R/W	A[5:2]		
BPI_DLL_Reset	W	0	rrrr	Resets the DLL's, which causes an asynchronous reset of the FPGA until the DLL's lock.
BPI_StatusA BPI_StatusB	R R	0 8	rDHS D = DPU bus fault H = BG bus header word fault S = BG bus stop word fault  The BG bus is the bus that carries data blocks from the transition module to the BPI FPGA.	Status bits. <b>The D bit</b> indicates that the value driven onto the DPU bus was not read back from the DPU bus, e.g., due to a short or bus contention. The D bit is cleared by reset or by disabling the DPU bus output via the BPI_DPU_BusControl register. <b>The H and S bits</b> indicate that an incorrect value was detected for a data block's header or stop word. The H and S bits are cleared by reset or by enabling the verifier via the BPI_VerifyMode register.
BPI_VerifyMode	R/W	1	rrMM MM = verify mode 00: verifier hold 01: verify with otestAlternate pattern 10: verify with otestCount pattern 11: verifier disabled	Control register for the Pattern Verifiers. The deserializers and data buffers are disabled except when MM = 11. Error counters are reset when MM goes from any value to 01 or 10. Error counters are not incremented when MM = 00. Error counters saturate at 0xffff.
BPI_VerifyResults	R/W	2	rrrr (write) any write loads the error counters into the readout shift register  VVVV (read) VVVV = four bits of error count	Register for reading out the two 16-bit Pattern Verifier error counters. <b>Writing to the register</b> loads the error counters into the readout shift register. This should only be done when verify mode is verifier hold. <b>Each subsequent read</b> reads out one nybble of the error counters in this order: side A MSN, ..., side A LSN side B MSN, ..., side B LSN
BPI_DPU_BusControl	R/W	3	AABB AA = control for side A bus to/from DPU BB = control for side B bus to/from DPU 00: output enabled, source is data buffer 01: output enabled, source is other data buffer 10: output enabled, source is other DPU bus 11: output disabled	Register that controls the operation of the two 25-bit busses between the BPI FPGA and its two DPU's. The four modes allow data to be routed: from either data buffer to either DPU from one DPU to the other DPU
BPI_TripletsL BPI_TripletsH	R/W R/W	4 5	LLLL rHHH HHLLLL = triplets per CTM data block	Number of triplets in each CTM data block.
BPI_BufferModeA BPI_BufferModeB	R/W R/W	6 7	rrMM MM = buffer mode 00: normal operation 01: HPU address mode 10: HPU write mode 11: HPU output trigger mode	Control registers for the data buffers. These registers are ignored when the Pattern Verifiers are enabled. During normal operation, the buffer data source is the deserializer. The other modes are used when the buffers are being written and controlled by the HPU. See BPI_BufferAccess.
BPI_BufferAccess	W	8	meaning depends on BPI_BufferMode	<b>In HPU address mode</b> , this register sets the 8-bit DPRAM line address: Paaaaaaa, where P is the page. The HPU writes the line address LS nybble first. Writing to the register also zeroes the line data nybble counters. <b>In HPU write mode</b> , the register is used to sequentially write nybbles of DPRAM input data. A line contains twelve nybbles. Once the HPU writes the twelfth nybble, the line is written to the DPRAM and the line address is incremented. <b>In HPU output trigger mode</b> , writing a zero triggers output of page 0, writing a one triggers output of page 1.
BPI_Test	R/W	f	TTTT	Standard test register. Writes write to the register. Reads read the register value and post-increment the value.

## TTC FPGA Registers

<i>In TTC FPGA, directly accessible:</i>	R/W	A[5:2]		
TTC_DLL_Reset	W	0	rrrr	Resets the DLL's (if any), which causes an asynchronous reset of the FPGA until the DLL's lock.
TTC_Status	R	0	Trrr5544 33221100 BABA BABABABA <-- side  T = TMP_N bit from transition module. 5-0 = BPI status summary bits.	<b>The TMP_N bit</b> is driven by the Power CPLD on the transition module (CTM). Its meaning is TBD. <b>The BPI status summary bits</b> are the OR of the status registers in the BPI FPGA's. There are two status summary bits per BPI FPGA, one for each of the FPGA's status registers.
TTC_TempVA TTC_TempVB TTC_TempBottom	R R R	1 2 3	rrrrrrrrr TTTTTTTT T = temperature in deg C <b>Temperature register values are only updated following a read of the TTC_Status register.</b>	Temperature register values are only updated following a read of the TTC_Status register. See temperature note. <b>The TempVA sensor</b> is ICU8, near the DSP core supply regulator (PWU9). <b>The TempVB sensor</b> is ICU9, near the FPGA core supply regulator (PWU10). <b>The TempBottom sensor</b> is ICU10, near the bottom edge of the board.
TTC_StatusMask	R/W	e	MrrrMMMM MMMMMMMM M = mask bit	A 1 in a mask bit enables the corresponding bit in TTC_Status to contribute to the interrupt line that interrupts the HPU.
TTC_Test	R/W	f	TTTTTTTTT TTTTTTTTT	Standard test register. Writes write to the register. Reads read the register value and post-increment the value.

The TTC FPGA is only used for temperature sensor readout, relaying of summary status information, etc.

### Temperature note:

The temperature sensors continuously perform temperature-to-digital conversions at a minimum rate of ~5 conversions/second. Accuracy is +/- 2 deg C. Though the sensors are capable of 12-bit (.0625 deg C) conversions, the current Verilog implementation provides an 8-bit (1 deg C) temperature reading.

The temperature registers are updated when the TTC\_Status register is read. Therefore, the TTC\_Status register should always be read out immediately prior to temperature register reads, e.g., with a DMA transfer that reads all four registers in turn.

