

ROD/ASM II Interface

I. The ROD transmits a clock and 17 parallel control bits to the ASM II via optical G-Link.

Clock: ~40 MHz (LHC BC clock)

Control Bits:

Name	Count	Description	Comment	Note
WA0-7	8	SCA Write Address	advances every other BC clock	1
WR_CLK	1	SCA Write Clock (20 MHz)		1
RD_CLK	1	SCA Read Clock = (6.67 MHz)		
GA0-1	2	SCA Channel Select		
RD	1	SCA Read address strobe		
SD	1	SCA Serial read address		
TX_DAV	1	per-word enable for G-Link transmitter	simplifies ROD/ASM II synchronization	
CAL	1	Calibration strobe		
DAC_CLK	1	clock for serial data into Calibration DAC		
DAC_D	*0	serial data for Calibration DAC	same as SD	2
ADC_ENCODE	*0	start conversion (ADC clock)	derived from RDCLK	2
SR_LOAD	*0	load ADC value into output shift register	derived from RDCLK	2
Total	17			

1. The LHC BC clock might be used as the SCA write clock. The SCA would see two write clocks per sample. The control bit allocated to WR_CLK could then be used for another purpose.
2. The older 1022/1024 G-Link chip set can transmit up to 21 bits plus clock. The newer 1032/1034 G-Link chip set uses less power than the older chip set but can transmit at most 17 bits plus clock. An ATLAS standard 220 mm transition module will need to use the 1032/1034 chip set to satisfy power constraints.

II. The ASM II transmits ADC data to the ROD via two optical G-Links operating at the beam clock rate.

Only digitized SCA samples are routinely transmitted. For example, data from ADC's dedicated to monitoring currents or temperature might be transmitted during a system-wide reset period using G-Link bits that are normally dedicated to transmitting SCA samples.

The G-Link word size is 16 bits, for a total of 32 bits per ASM II. Two bits are dedicated to each of the 16 main ADC's on the ASM II. There are no framing bits, CRC bits, etc. There is no means of detecting bit errors in the data. Synchronization is established via the TX_DAV mechanism as shown in the "ROD-ASM II Interaction" diagram appended to this document.

III. If required by the ASM II design, the ROD helps the ASM II establish/reestablish G-Link lock.

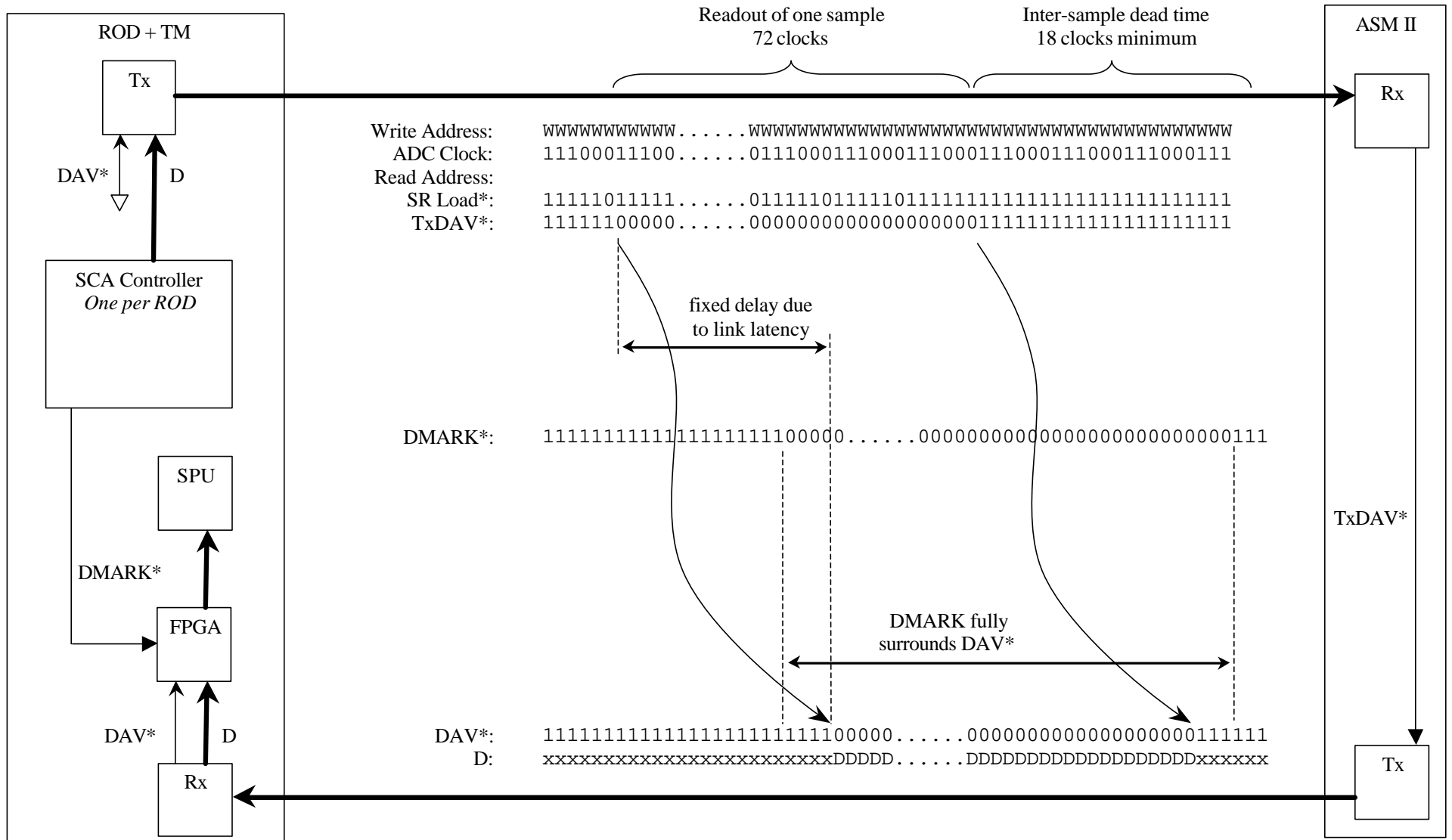
The G-Link receiver on the ASM II needs a reference frequency to establish lock. This reference frequency can come from a local source on the ASM II, such as a crystal oscillator, or from the ROD via the optical fiber. If there is no local crystal oscillator on the ASM II, then the ROD must transmit an Idle Word to an ASM II if it sees that both data links for the ASM II are out of lock. The Idle Word's bit pattern creates a clock at the word rate. The ASM II must provide a mechanism to use this clock as the reference clock until frequency lock is obtained. The 1024 G-Link receiver has this mechanism built in. The 1034 does not.

IV. Laser Safety.

If laser safety is determined to be a concern, the ROD and ASM II will have the responsibilities listed below, which ensure that lasers are disabled if an entire optical cable is severed. For example, all the optical fibers for a single chamber may be carried in a single cable.

The ASM II must disable its lasers whenever its clock/control link is out of lock. This rule can be implemented with little or no additional circuitry on the ASM II and assumes that data and clock/control fibers for an ASM II are in the same cable.

The ROD must disable all of the lasers it drives into a cable under certain conditions (to be determined). For example, if several data links within a single cable cannot retain or establish lock, then the ROD must disable all lasers it drives into that cable.



Notes:

1. DMARK* is a signal dedicated to notifying the FPGA when it should expect to see data arriving on the G-Link. It need not be precisely timed, because the G-Link Rx outputs a DAV* signal to the FPGA.
2. The FPGA reformats the data stream, removes dead words, and tags the first time slice of each event.