

ROD Slot Pinout for ATLAS Muon CSC (Preliminary)

Features:

Off-the-shelf VME64x J1/J0/J2 backplane is OK for ROD.

Notes:

TIM = TTC Interface Module (the crate's interface to the TTC).

ROD's mate with slot connectors installed in front of the backplane.

Transition modules (back-of-crate cards) mate with slot connector pins protruding behind the backplane.

Non-VME Signals are active high unless noted otherwise.

'3V' levels are TTL compatible; '3V' is used to remind designers of issues associated with powering some chips from 5V and others from 3.3V.

Each slot receives a single differential PECL clock signal (TCLKI), which can be shared by both the ROD and the back-of-crate card.

The clock signal is terminated on the ROD; bussed signals are terminated on the backplane.

Explanation of Backplane column:

pass-thru = the signal is connected between a ROD and its back-of-crate card with no connection made to the backplane

bussed = (see 'Variations') all ROD and TIM slots are connected together on the backplane either via traces or power/ground planes

pt-to-pt = traces on the backplane form separate point-to-point connections between ROD slots and dedicated TIM pins

hardwired = signals are hard-wired either high or low on the backplane

Pin Counts and Connector Assignments

User-defined Signals	Symbol	Level	Backplane	Pin Count					Total	
				J6/P6	J5/P5	J2/P2	J0/P0	J1/P1		
Generic FPGA connections										
TTC (active low, from TIM slot)	TG0-TG7	3V	bussed	8						8
TTC FPGA additional	TG8-TG15	3V	pass-thru	8						8
BPI FPGA's	BG_...	3V	pass-thru	80	72	40				192
DXD FPGA	DG0-DG56	3V	pass-thru				57			57
JTAG and FPGA Configuration	misc.	3V	pass-thru			8				
RESET_N (output by ROD)	RESET_N	3V	pass-thru			1				
Clocks										
RCLKI (input to ROD)	RCLKI	dif	pass-thru		2					2
TCLKI (input to ROD)	TCLKI	dif	pt-to-pt	2						2
DCLKO (output by ROD)	DCLKO	LVDS	pass-thru				2			2
RCLKO (output by ROD)	RCLKO	LVDS	pass-thru		2					2
SCLKO (output by ROD)	SCLKO	LVDS	pass-thru		2					2
TCLKO (output by ROD)	TCLKO	LVDS	pass-thru		2					2
Busy (active low, to TIM slot)	BUSYN	3V	pt-to-pt		1					1
User-defined Signal Subtotal				98	81	49	59	0		287

Additional Power/Ground	Symbol	Level	Backplane	Pin Count					Total	
				J6/P6	J5/P5	J2/P2	J0/P0	J1/P1		
+5V	P5V		bussed	2	6					8
+3.3V	P3V		bussed	6	6					12
V1 and V2 to transition module							4			
Pass-thru ground	PTGND		pass-thru			49	30			79
Ground	GND		bussed	19	17					36
Additional Power/Ground Subtotal				27	29	49	34	0		139

Max Current @
1.25 A per pin

10.00
15.00

VME64x	Symbol	Level	Backplane	Pin Count					Total	Max Current @ 1.25 A per pin	
				J6/P6	J5/P5	J2/P2	J0/P0	J1/P1			
GA	GA0-GA4,GAP		hard-wired			0		6	6		
unused user-defined VME/VME64x	spare		pass-thru	0	0	12	2	0	14		
miscellaneous VME			bussed			25		83	108		
miscellaneous VME64x			bussed			1		30	31		
+5V	P5V		bussed			3		3	6	7.50	
+3.3V	P3V		bussed			0		10	10	12.50	
+12V, -12V			bussed			0		2	2	2.50	
Shield	SHLD		bussed	25	22	0	19	0	66		
Ground	GND		bussed			20		24	44		
Mate-first-break-last ground	MFBLGND		bussed			1		2	3		
VME64x Subtotal				25	22	62	21	160	290		

Grand Totals	Pin Count					Total	Max Current @ 1.25 A per pin	
	J6/P6	J5/P5	J2/P2	J0/P0	J1/P1			
Total Pins Used	150	132	160	114	160	716		
Total Pins Available (including shield "pins")	150	132	160	114	160	716		
Total +5V	2	6	3	0	3	14	17.50	
Total +3.3V	6	6	0	0	10	22	27.50	
Total +5V excluding J1/P1						11	13.75	
Total +3.3V excluding J1/P1						12	15.00	

Signal and Grounding Summary	J6/P6	J5/P5	J2/P2	J0/P0	J1/P1	Total
Total Signals (excluding unused user-defined signals and some DC signals)	98	81	75	59	113	426
Total Grounds	19	17	70	30	26	162
Total Shields	25	22	0	19	0	66
Total +5V, +3.3V	8	12	3	0	13	36
Signal to Ground Ratio	5.16	4.76	1.07	1.97	4.35	2.63
Signal to (Ground + +5V + +3.3V) Ratio	3.63	2.79	1.03	1.97	2.90	2.15
Signal to (Shield+Ground) Ratio	2.23	2.08	1.07	1.20	4.35	1.87
Signal to (Shield+Ground + +5V + +3.3V) Ratio	1.88	1.59	1.03	1.20	2.90	1.61

Notes

3V = 3.3V CMOS levels.

dif = wide-common-mode differential, compatible with LVDS, dif PECL, dif ECL

Some 3.3V devices may have +/- 5% supply tolerances, hence the many P3V pins:

$$1.25A * 50 \text{ mohm} = 63 \text{ mV}$$

$$3.3V * 5\% = 165 \text{ mV}$$

One row of shield "pins" is assumed for those connectors that have shields.

J6/P6 is a Type B connector (no central multifunction block).

Pass-thru ground is connected to the back-of-crate and ROD digital ground planes but not to the backplane ground plane.

J4/P4 is not implemented; the J4/P4 area is used for bus bars.

If a full-custom 9U backplane is designed:

pass-thru grounds become standard grounds (i.e., they are connected to the backplane ground plane(s),
the proposed bus bar arrangement may change.

Pin Assignments

J0/P0:	a	b	c	d	e	f	Counts		
							GND	DG	other
1	GND	NEGV2	NEGV1	POSV2	POSV1	shld	1	0	0
2	GND	GND	GND	GND	GND	shld	5	0	0
3	DG	DG	DG	DG	DG	shld	0	5	0
4	GND	DG	DG	DG	DG	shld	1	4	0
5	DG	GND	DG	GND	DG	shld	2	3	0
6	GND	DG	DG	DG	DG	shld	1	4	0
7	DG	DG	GND	DG	GND	shld	2	3	0
8	GND	DG	DG	DG	DG	shld	1	4	0
9	DG	GND	DG	GND	DG	shld	2	3	0
10	GND	DG	DG	DG	DG	shld	1	4	0
11	DG	DG	GND	DG	GND	shld	2	3	0
12	GND	DG	DG	DG	DG	shld	1	4	0
13	DG	GND	DG	GND	DG	shld	2	3	0
14	GND	DG	DG	DG	DG	shld	1	4	0
15	DG	DG	GND	DG	GND	shld	2	3	0
16	spare	DG	DG	DG	DG	shld	0	4	0
17	GND	GND	DG	GND	DG	shld	3	2	0
18	DCLKOP	GND	DG	DG	DG	shld	1	3	0
19	DCLKON	GND	spare	DG	GND	shld	2	1	0
							30	57	0
should be:							30	57	0

italics indicate VME-defined pins

J2/P2:	z	a	b	c	d	Counts		
						GND	BG	other
1	spare	spare	<i>P5V</i>	spare	spare	0	0	0
2	<i>GND</i>	<i>GND</i>	<i>GND</i>	<i>GND</i>	spare	4	0	0
3	spare	<i>GND</i>	<i>retry*</i>	<i>GND</i>	spare	2	0	0
4	<i>GND</i>	TMS	<i>A24</i>	<i>GND</i>	<i>GND</i>	3	0	0
5	BG	<i>GND</i>	<i>A25</i>	<i>GND</i>	BG	2	2	0
6	<i>GND</i>	TDI	<i>A26</i>	<i>GND</i>	BG	2	1	0
7	BG	<i>GND</i>	<i>A27</i>	<i>GND</i>	BG	2	2	0
8	<i>GND</i>	TDO	<i>A28</i>	<i>GND</i>	BG	2	1	0
9	BG	<i>GND</i>	<i>A29</i>	<i>GND</i>	BG	2	2	0
10	<i>GND</i>	TCK	<i>A30</i>	<i>GND</i>	BG	2	1	0
11	BG	<i>GND</i>	<i>A31</i>	<i>GND</i>	BG	2	2	0
12	<i>GND</i>	spare	<i>GND</i>	<i>GND</i>	BG	3	1	0
13	BG	<i>GND</i>	<i>P5V</i>	<i>GND</i>	BG	2	2	0
14	<i>GND</i>	spare	<i>D16</i>	<i>GND</i>	BG	2	1	0
15	BG	<i>GND</i>	<i>D17</i>	<i>GND</i>	BG	2	2	0
16	<i>GND</i>	CCLK	<i>D18</i>	<i>GND</i>	BG	2	1	0
17	BG	<i>GND</i>	<i>D19</i>	<i>GND</i>	BG	2	2	0
18	<i>GND</i>	DIN	<i>D20</i>	<i>GND</i>	BG	2	1	0
19	BG	<i>GND</i>	<i>D21</i>	<i>GND</i>	BG	2	2	0
20	<i>GND</i>	PROG0_N	<i>D22</i>	<i>GND</i>	BG	2	1	0
21	BG	<i>GND</i>	<i>D23</i>	<i>GND</i>	BG	2	2	0
22	<i>GND</i>	PROG1_N	<i>GND</i>	<i>GND</i>	BG	3	1	0
23	BG	<i>GND</i>	<i>D24</i>	<i>GND</i>	BG	2	2	0
24	<i>GND</i>	spare	<i>D25</i>	<i>GND</i>	BG	2	1	0
25	BG	<i>GND</i>	<i>D26</i>	<i>GND</i>	BG	2	2	0
26	<i>GND</i>	spare	<i>D27</i>	<i>GND</i>	BG	2	1	0
27	BG	<i>GND</i>	<i>D28</i>	<i>GND</i>	BG	2	2	0
28	<i>GND</i>	TMP_N	<i>D29</i>	<i>GND</i>	BG	2	1	0
29	BG	<i>GND</i>	<i>D30</i>	<i>GND</i>	BG	2	2	0
30	<i>GND</i>	RESET_N	<i>D31</i>	<i>GND</i>	BG	2	1	0
31	BG	<i>GND</i>	<i>GND</i>	<i>GND</i>	<i>GND</i>	4	1	0
32	<i>GND</i>	<i>GND</i>	<i>P5V</i>	<i>GND</i>	<i>VPC</i>	3	0	0
should be:						70	40	0
should be:						70	40	0

TMP_N = Transition Module Present,
pulled high on ROD, grounded on TM

J5/P5:	a	b	c	d	e	f	Counts		
							GND	BG	TG
1	RCLKIP	RCLKOP	SCLKOP	TCLKOP	GND	shld	1	0	0
2	RCLKIN	RCLKON	SCLKON	TCLKON	GND	shld	1	0	0
3	GND	GND	GND	GND	BUSYN	shld	4	0	0
4	BG	BG	GND	BG	BG	shld	1	4	0
5	BG	BG	BG	BG	BG	shld	0	5	0
6	BG	P5V	BG	BG	GND	shld	1	2	0
7	BG	P5V	BG	BG	BG	shld	0	3	0
8	BG	P5V	GND	BG	BG	shld	1	2	0
9	BG	P5V	BG	BG	BG	shld	0	3	0
10	BG	P5V	BG	BG	GND	shld	1	2	0
11	BG	P5V	BG	BG	BG	shld	0	3	0
12	BG	BG	GND	BG	BG	shld	1	4	0
13	BG	BG	BG	BG	BG	shld	0	5	0
14	GND	BG	BG	BG	GND	shld	2	3	0
15	BG	BG	BG	BG	BG	shld	0	5	0
16	BG	BG	GND	BG	BG	shld	1	4	0
17	BG	P3V	BG	BG	BG	shld	0	3	0
18	BG	P3V	BG	BG	GND	shld	1	2	0
19	BG	P3V	BG	BG	BG	shld	0	3	0
20	BG	P3V	GND	BG	BG	shld	1	2	0
21	BG	P3V	BG	BG	BG	shld	0	3	0
22	BG	P3V	BG	BG	GND	shld	1	2	0
							17	60	0
should be:							17	72	0

J6/P6:	a	b	c	d	e	f	Counts		
							GND	BG	TG
1	BG	BG	BG	BG	BG	shld	0	5	0
2	BG	BG	GND	BG	BG	shld	1	4	0
3	BG	BG	BG	BG	BG	shld	0	5	0
4	GND	BG	BG	BG	GND	shld	2	3	0
5	BG	BG	BG	BG	BG	shld	0	5	0
6	BG	BG	GND	BG	BG	shld	1	4	0
7	BG	BG	BG	BG	BG	shld	0	5	0
8	GND	BG	BG	BG	GND	shld	2	3	0
9	BG	BG	BG	BG	BG	shld	0	5	0
10	BG	BG	GND	BG	BG	shld	1	4	0
11	BG	BG	BG	BG	BG	shld	0	5	0
12	GND	BG	BG	BG	GND	shld	2	3	0
13	BG	BG	BG	BG	BG	shld	0	5	0
14	BG	BG	GND	BG	BG	shld	1	4	0
15	BG	BG	BG	BG	BG	shld	0	5	0
16	BG	TG15	TG14	BG	GND	shld	1	2	2
17	GND	GND	TG13	BG	BG	shld	2	2	1
18	TG7	P3V	TG12	GND	BG	shld	1	1	2
19	TG6	P3V	TG11	BG	BG	shld	0	2	2
20	TG5	GND	TG10	BG	GND	shld	2	1	2
21	TG4	P3V	TG9	BG	BG	shld	0	2	2
22	TG3	P3V	TG8	BG	BG	shld	0	2	2
23	TG2	GND	GND	GND	BG	shld	3	1	1
24	TG1	P3V	TCLKIP	P5V	BG	shld	0	1	1
25	TG0	P3V	TCLKIN	P5V	BG	shld	0	1	1
							19	80	16
should be:							19	80	16

TG0-TG7 are bussed on the backplane;
their positions are influenced by TIM slot pinout

For detailed BG and DG pinouts, see !!!