

CSC Off-Detector Electronics Power Considerations, 9U subrack

Occupied VMEbus slots per subrack	18		
Transition modules per subrack	16		
	400	220	120
	mm	mm	mm
	TM	TM	TM

ATLAS Power Supply Limitations:

<b>3.3V supply current</b>	<b>200</b>	<b>200</b>	<b>200</b>	<b>A/subrack</b>
<b>5.0V supply current</b>	<b>300</b>	<b>300</b>	<b>300</b>	<b>A/subrack</b>
3.3V supply current	11.1	11.1	11.1	A/slot
5.0V supply current	16.7	16.7	16.7	A/slot
3.3V supply power	36.7	36.7	36.7	W/slot
5.0V supply power	83.3	83.3	83.3	W/slot
Power per slot	120.0	120.0	120.0	W/slot

ATLAS Cooling Limitations

<b>Transition module power</b>	<b>70</b>	<b>39</b>	<b>21</b>	<b>W/TM</b>
<b>VMEbus module power</b>	<b>110</b>	<b>110</b>	<b>110</b>	<b>W/VMEbus module</b>
Power per slot	180	149	131	W/slot

DSP module count	13			DSP/ROD	
ROD Motherboard FPGA count	10			FPGA/ROD	
ASM's serviced per Transition Module	10			ASM/TM	
TM FPGA count	10			FPGA/TM	
serializer power dissipation	0.255			W/serializer	power for 1 MGT even though RX is not used
deserializer power dissipation	0.255			W/serializer	power for 1 MGT even though TX is not used

	<u>w/o inefficiency</u>			<u>efficiency</u>	<u>w/ inefficiency</u>			
	<u>3.3V</u>	<u>5V</u>	<u>total</u>		<u>3.3V</u>	<u>5V</u>	<u>total</u>	
<b>ROD DSP Modules</b>								
DSP core power (300 MHz 6203)		1.5		93%	0.0	1.6		W/DSP
DSP I/O power	0.3			100%	0.3	0.0		W/DSP
FPGA internal power		0.5		93%	0.0	0.5		W/DSP
FPGA I/O power	0.3			100%	0.3	0.0		W/DSP
subtotal per ROD	7.8	26.0	33.8		7.8	28.0	35.8	W/ROD
<b>ROD Motherboard FPGA's</b>								
FPGA internal power		0.5		93%	0.0	0.5		W/FPGA
FPGA I/O power	0.3			100%	0.3	0.0		W/FPGA
subtotal per ROD	3.0	5.0	8.0		3.0	5.4	8.4	W/ROD
<b>ROD Motherboard Other</b>								
PLD's	1.0			100%	1.0	0.0		W/ROD
VME buffers		1.0		100%	0.0	1.0		W/ROD
Clock Generation	1.0	1.4		100%	1.0	1.4		W/ROD
FIFO's	0.3			100%	0.3	0.0		W/ROD
DPRAM's	0.1			100%	0.1	0.0		W/ROD
buffers	1.0			100%	1.0	0.0		W/ROD
subtotal per ROD	3.5	2.4	5.9		3.5	2.4	5.9	W/ROD
<b>TM Analog Supply efficiency 78%</b>								
<b>TM Links to/from ASM</b>								
optical transmitter (one 12-fiber module)	1.1			100%	1.1	0.0		W/TM
optical receivers (two 12-fiber modules)	2.6			100%	2.6	0.0		W/TM
calibration serializers (two MGT Tx's)		0.5		78%	0.0	0.7		W/TM
monitor deserializers (two MGT Rx's)		0.5		78%	0.0	0.7		W/TM
serializer (one MGT Tx)		0.3		78%	0.0	0.3		W/ASM
deserializers (two MGT Rx)		0.5		78%	0.0	0.7		W/ASM
subtotal per Transition Module	3.7	8.2	11.9		3.7	11.1	14.8	W/TM
<b>TM other</b>								
S-Link	7.5			100%	7.5	0.0		W/SLINK
FPGA internal power (1.5V)		1.0		90%	0.0	1.1		W/FPGA
FPGA aux power (2.5V)		0.5		78%	0.0	0.7		W/FPGA
FPGA I/O power		0.2		78%	0.0	0.3		W/FPGA
subtotal per Transition Module	7.5	17.4	24.9		7.5	20.6	28.1	W/TM

<b>Power:</b>					<b>3.3V</b>	<b>5V</b>	<b>total</b>	
ROD Total	14.3	33.4	47.7		14.3	35.7	50.0	W/ROD
TM Total	11.2	25.6	36.8		11.2	31.7	42.9	W/TM
Grand Total	25.5	59.0	84.4	91%	25.5	67.4	92.9	W/slot
Max allowed					36.7	83.3	120.0	W/slot (limited by power supply current rating)

<b>Current:</b>					<b>3.3V</b>	<b>5V</b>	<b>total</b>	
ROD Total					4.3	7.1		A/ROD
TM Total					3.4	6.3		A/TM
Grand Total					7.7	13.5		A/slot
Max allowed					11.1	16.7		A/slot (limited by power supply current rating)

**Power Pins:**

	<b>3.3V</b>	<b>5V</b>	<b>total</b>	
ROD: VME backplane	10	6		pin/ROD
ROD: J5/J6 backplane	12	8		pin/ROD
TM: VME backplane	0	3		pin/TM
TM: J5/J6 backplane	12	8		pin/TM
ROD: total	22	14		pin/ROD
TM: total	12	11		pin/TM