

**ROD Hardware Design Tasks**

What	Priority	Who	% Complete	Working Prototype?
<b>PCB Design and Layout Data Entry</b>				
GPU (DSP Module)	-	Nigel, Steve	100%	yes
GPU Test Board	-	Nigel, Steve	100%	yes
ROD Motherboard	-	Nigel, Steve	100%	yes
ROD TM	med	Steve	0%	no
J5/J6 Backplane	low	Steve or TBD	0%	no
<b>ROD CPLD Verilog Coding</b>				
Host	-	Nigel	99%	yes
Flash	-	Nigel	99%	yes
VMEC	-	Nigel	95%	yes
VMED	-	Baruch	100%	yes
Noisy (clock generation)	-	Michael M	75%	yes
Quiet (clock generation)	-	Michael M	75%	yes
<b>ROD and TM FPGA Verilog Coding</b>				
TTC (SCA control, etc.)	med	Steve or TBD	0%	no
BPI	med-high	Michael M	50%	no
DC	low	Nigel, TBD	30%	no
DPU EMIF	high	Nigel, Steve	50%	no
HPU EMIF	-	Steve	80%	yes
HPU XB	-	Steve	50%	yes
SPU XB	med	Steve or TBD	0%	no
RPU XB	low	Steve or TBD	0%	no
DXF	high	Nigel	95%	no
DXB	low	Steve or TBD	0%	no
TM FPGA's	med	Steve or TBD	0%	no
<b>ROD Testing in Addition to Above</b>				
Power switching, startup sequence	-	Steve	50%	yes
Overvoltage protection	low	Steve	30%	yes
Clock Generation functionality	high	Steve, Michael M	20%	yes
Clock signal integrity	-	Steve	50%	yes
Boot flash memory functionality	-	Steve, Michael M	80%	yes
VME dual-port RAM	-	Steve	80%	yes
JTAG CPLD programming	-	Nigel, Steve	90%	yes
DSP in-system emulation	-	Steve	50%	yes
Front-panel switches and indicators	-	Steve	80%	yes
HPU boot	-	Steve	90%	yes
DPU boot	high	Steve	0%	no
<b>ROD Reference/User Manual</b>				
	med	Steve	10%	no

Reminder: Off-detector electronics development is scheduled in three phases: Prototype, Module 0, Production. We hope to avoid redesign of hardware in the Module 0 and Production phases.

**ROD Software Tasks**

What	Priority	Who	% Complete	Working Prototype?
<b>HPU</b>				
Low-level Drivers				
System Initialization	low	Steve or TBD	10%	no
Clock Generation	high	Michael M	75%	no
temperature monitoring	low	TBD	0%	no
power monitoring	low	TBD	0%	no
Decoder Control	low	Steve	10%	no
Data Exchange	high	Steve	10%	no
Interconnect	med	TBD	0%	no
FPGA configuration	high	Michael M	95%	no
<b>HPU high-level code</b>				
conceptual design	high	Steve	80%	-
run code	low	TBD	10%	no
calibration code	low	TBD	0%	no
model for Trigger/DAQ (RCC) interface	low	Steve	75%	-
<b>SPU</b>				
run code				
conceptual design	high	Donovan	ask	-
C	ask	Donovan	ask	no
assembly	ask	Donovan	ask	no
test code (data source in ROD self-test)	ask	Donovan	ask	
<b>RPU</b>				
run code				
conceptual design	high	Michael S	ask	-
C	ask	Michael S	ask	simulated
assembly, if any	ask	Michael S	ask	-
test code (data source in ROD self-test), if any	ask	Michael S	ask	-
<b>Other</b>				
Secondary boot loader	high	Steve	90%	no
ROD control panel (GUI)	low	Steve, Michael M	20%	yes
ROD Software Reference/User Manual	low	Steve or TBD	0%	no

**Dedicated Test Software, not indicated above, is needed:**

to test Hardware

  to test/diagnose Hardware during hardware development

  to test/diagnose Hardware during production

    GPU self test

    ROD self test

    TM self test

  to test/diagnose Hardware during installation/commissioning

    GPU in situ self test

    ROD in situ self test

    TM in situ self test (?)

to test Software

  to test Software during software development

  to test/diagnose Software during installation/commissioning

**GPU Evaluation**

What	Priority	Who	% Complete	Working Prototype?
<b>Hardware</b>				
Test board assembly	-	Nigel, Steve	100%	yes, 2
GPU assembly	-	Nigel, Steve	100%	yes, 2
XFGPA Verilog: reset, reset straps	-	Nigel	90%	yes
EFGPA Verilog: generics, synthesizers, boot	-	Nigel	90%	yes
<b>Software</b>				
communication between XFGPA, EFGPA	-	Nigel	100%	yes
generics exercise	-	Nigel	90%	yes
SDRAM test	-	Nigel	90%	yes
clock synthesizer setup	-	Nigel	100%	yes
temp sensor readout	-	Nigel	100%	yes
serial number readout	low	TBD	0%	no

**Other**

What	Priority	Who	% Complete	Working Prototype?
Thermal Profile for BGA connector	-	Steve	90%	yes
<b>Purchasing</b>				
GPU parts		Steve	99%	-
DSP Test Board parts		Steve	100%	-
ROD Motherboard parts		Steve	100%	-
ROD TM parts	med	TBD	0%	-
J5/J6 backplane parts	low	TBD	0%	-

Priority key:

- high = the item is at the top of the to-do list
- med = the item is simmering on the back burner
- low = the item is nonessential for some time to come
- = the existing prototype is adequate for some time to come
- ask = ask the responsible person