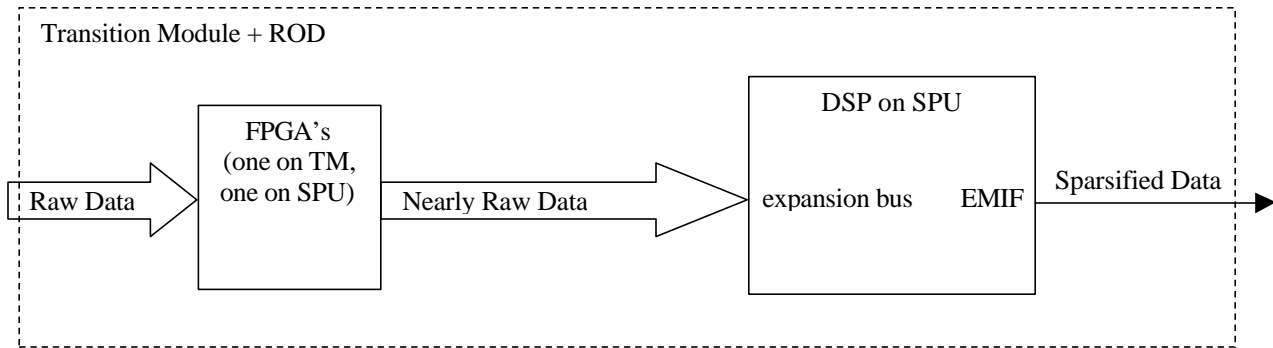


CSC ROD Wish List for On-Chamber Electronics

Introduction

A wish list for on-chamber electronics appears below. These wishes are influenced by the cost and complexity issues associated with the DSP-based sparsification solution, and to a large extent any solution. The diagram below shows the TM + ROD data path and some of the critical issues associated with it. A diagram of the data section of the TM + ROD appears on the second page of this document.

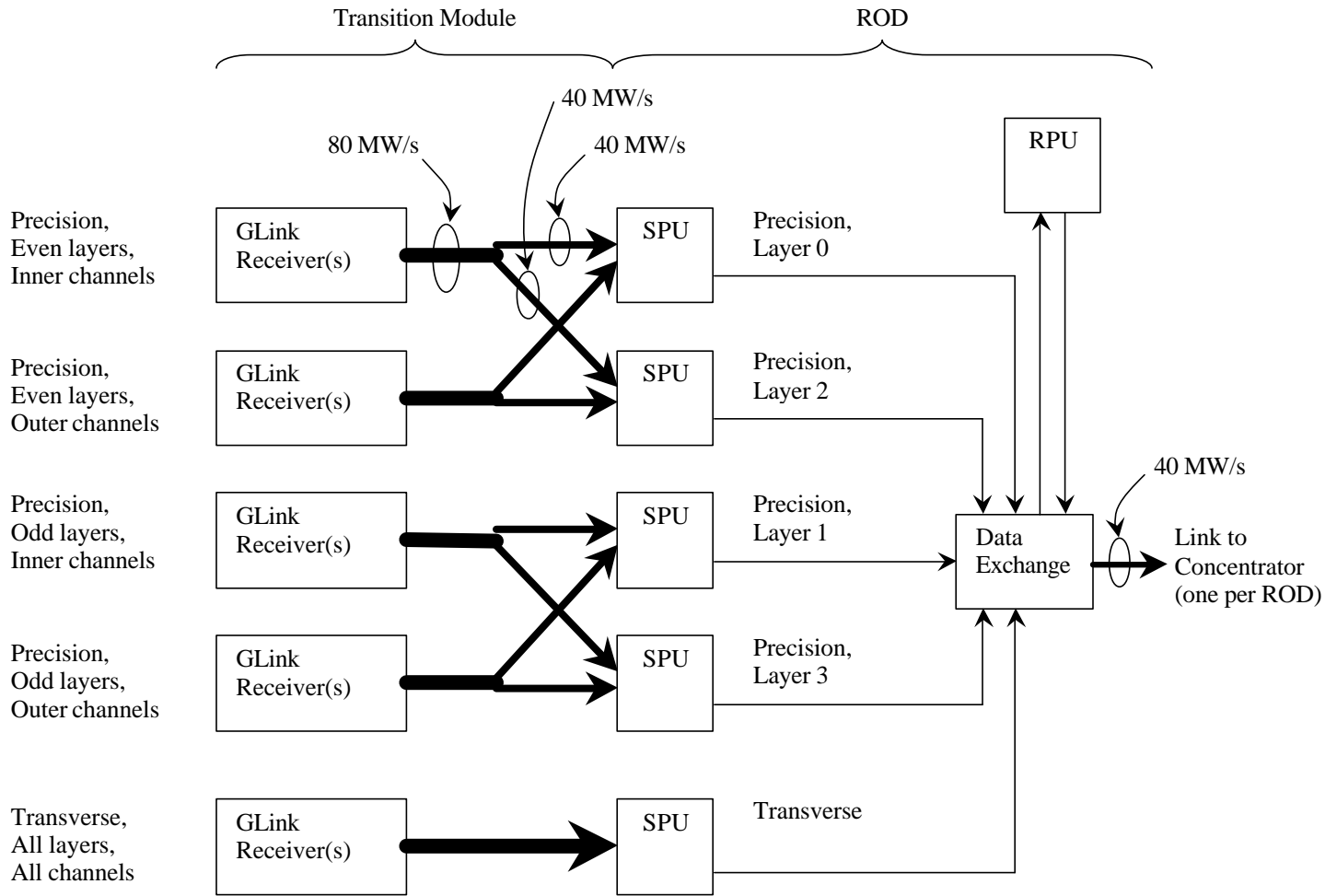


Critical issues: *FPGA complexity* *DSP Input Bandwidth* *DSP Processing Power*
 FPGA buffering capacity

	Wish	Why
1.	The ASM should avoid multiplexing data from different layers onto a single HDMP-1022 data line. The best scenario for the Sparisifier is one or two HDMP-1022 data lines being dedicated to each ADC.	The ROD will work most efficiently if each DSP handles one layer (except transverse). If a single HDMP-1022 data line carried data from two layers, the data line would need to be routed to two DSP modules and the FPGA on each module would have to extract the data needed by that module.
2.	If two data G-Links are used per ASM, the ASM should dedicate one G-Link to each layer (two layers for transverse).	If a G-Link carried data from two layers, data from both layers would be affected if the link went down. Also, a DSP probably cannot operate on partial data from a layer, so a single down link would result in a loss of all data from the ASM.
3.	The ASM should output channels in a reasonable order. The best order is 0, 1, 2, ... 191.	The DSP algorithms will be more efficient if channels are in a reasonable order. The FPGA can only perform minor reordering, for example, reordering channels within an ADC (which would require at most a 12x4-bit lookup table).
4.	The ASM should output non-channel data, e.g., from monitoring ADC's, in a manner consistent with output of channel data.	The FPGA design will be greatly simplified if non-channel data can be handled in a manner similar to channel data.
5.	The ASM should send only useful data and padding words. (It should use the DAV* input on the HDMP-1022 to suppress useless words).	The FPGA design will be greatly simplified if the FPGA does not examine the data passing through it. DSP input bandwidth is also a concern.
6.	If the ASM uses two 40 MW/s HDMP-1022 transmitters, the word size should be 16 bits.	The low-power HDMP-1034 is compatible with the HDMP-1022 if the word size is 16 bits. The HDMP-1034 is needed to minimize ROD power dissipation.
7.	(ASM data G-Links can be 40 MW/s or 80 MW/s, provided it is determined that the chips reliably operate at 80 MW/s.)	The FPGA will be able to handle 80 MW/s.
8.	(ASM readout can be on a per-time-slice basis, rather than a per-trigger basis.)	The DSP will handle caching of overlapping time slices.

A note on the time slices to be read out: This wish list assumes an ASM which is read out on a per-time-slice basis rather than a per-trigger basis. The number of time slices to be read out and their temporal relationship (e.g., consecutive or not) are not directly addressed. Nonetheless, the ROD design can place restrictions on the choice of time slices, especially at a L1 rate of 100 kHz. Most development work to date has assumed four consecutive time slices.

TM + ROD Data Paths with Preferred Raw Data Connections



Notes:

- Most of the above is duplicated for the second chamber serviced by the ROD.
- Rates are link bandwidths, not data rates.
- W = 16-bit word.