

I. General Notes

The CSC ROD Backplane (CRB) is a mostly passive circuit board intended to be mounted in the J5/J6 area of a 9U VME64x subrack.

The design was captured with C++. There are no schematics. The files listed below are available here:

<http://positron.ps.uci.edu/~pier/csc/sup/Support.html>

file/folder name	description
CRB_LayoutNotes0.doc	this file
CRB_BOM_for_layout0.xls	Excel file containing a bill of materials annotated for PCB layout
CRB_PowerAndMech_01.xls	Excel file containing power calculations and a mechanical overview.
CRB_PP_Netlist.txt	the CRB's CAD netlist in PADS PowerPCB format (an Allegro netlist can also be generated)
CRB_View1.html	the CRB's symbolic netlist

II. Notes on C++ Design Capture

These notes are provided as an aid to understanding the symbolic netlist. It may be necessary to consult the symbolic netlist when implementing the layout notes in this document. For example, to properly place decoupling capacitors, VCC pins must be distinguished from unused input pins tied to VCC. The CAD netlist does not contain pin functionality information.

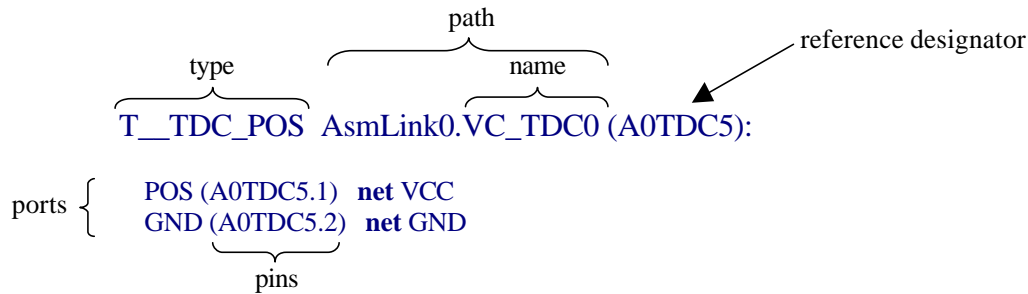
A design captured in C++ contains the following:

Subsystems	Subsystems are the highest level modules. They are similar to the highest level pages of a schematic. The subsystems of the CRB are listed in a table below.
Modules	A module is a group of parts and any nets between their pins. A module is similar to a page of a schematic.
Parts	A part is a physical component like a resistor, a connector, or an integrated circuit. Parts are discussed more below.
Nets	A net is a set of part pins that are electrically connected. Each net has a unique name. The net named "/NC" is the no-connect net. The no-connect net appears in the symbolic netlist, but it is not included in the CAD netlist.

Every part has the following:

A type	Part types start with T followed by two underscores, e.g., T__74ALS00.
A name	Unlike parts in schematics, each C++ part has a meaningful symbolic name. For example, a resistor that is used as a series terminator might have a name like STerm. Part names are not unique within a design, because parts in separate modules might have the same name.
A path	The path fully describes a part's location within a design. It is a hierarchical list of modules followed by the part's name. For example, "Power.SW_VCC.Switch0" is the path of a part (Switch0) within the SW_VCC module within the Power module. Paths are unique within a design.
A reference designator	The reference designator is similar to schematic reference designators. It contains a little more information, as described below.
One or more ports	Ports are like symbolic part pins. There are three types of ports: single-wire -- one signal with one physical pin multi-pin -- one signal with two or more physical pins (example: ground pins) multi-wire -- two or more signals, each with one physical pin (example: pins of a data bus)
One or more pins	A pin represents a single physical pin of a part. Each pin is associated with a port.

This excerpt from a symbolic netlist shows a tantalum decoupling capacitor and its connections:



Reference Designators:

All reference designators consist of a base, a string, and a number. The string and number are similar to those in a standard schematic reference designator. The base identifies the subsystem in which the part is located. When a design contains two or more subsystems that are identical (i.e., they are the same type of module), the corresponding reference designators within these subsystems are identical except for the base. For example, A0U1 and A1U1 are the reference designators of two corresponding parts in separate identical subsystems.

Example reference designators from a symbolic netlist:

A0TDC5	-- a tantalum decoupling capacitor in the AsmLink[0] subsystem
A0U1	-- an integrated circuit in the AsmLink[0] subsystem
A1U1	-- an integrated circuit in the AsmLink[1] subsystem
A1RP2	-- a resistor pack in the AsmLink[1] subsystem
PWH1	-- a header in the Power subsystem

The CRB Subsystems table lists the bases for each CRB subsystem.

III. CRB Subsystems

The CRB has nineteen subsystems:

Subsystem	Reference designator base(s)	Description
RodSlot (x16)	R05-R12, R14-R21	one subsystem per ROD slot
TimSlot	T13	one subsystem for the TIM slot
Terminators	TM	terminators for bussed signals
Power	PW	power and mechanical components

The reference designator base for each slot contains its slot number (05-21). The CRB_PowerAndMech_01.xls spreadsheet shows the general arrangement of the slots.

IV. Common Abbreviations

CDC	ceramic decoupling capacitor, always place these near component power supply pins
TDC	tantalum decoupling capacitor
STerm	series terminating resistor, always place these near the driver
PTerm	parallel terminator resistor, always place these at the end of the transmission line, opposite the driver
DTerm	differential terminator resistor, always place these near the receiver
OSC	oscillator
MUX	multiplexer
GND	ground
NC, /NC	no-connect
_N	Used at the end of a port name or net name to indicate that the signal is active-low. Also used to indicate the active-low signal of a differential pair.
_P	Used to indicate the active-high signal of a differential pair
>>>	Used in the C++ source files to indicate important comments, especially PCB layout notes.

V. Board Notes

The CRB should conform to VME64x mechanical specifications. To determine mechanical dimensions:

consult IEEE 1101.1, IEEE 1101.10, IEEE 1101.11, VITA 1.1-199x, VITA 1.3 - 199x & VITA 23 - 199x, etc.,
consult <http://ess.web.cern.ch/ESS/crateProject/index.htm>, or
consult other LHC groups, e.g., the ATLAS liquid argon calorimeter group.

If a password is needed for the link above, contact UCI.

To match specified connectors (see bill of materials), the board thickness must be 5.2 +/- .3 mm.

***** **Plane layers must be 2 oz Cu, minimum.** *****

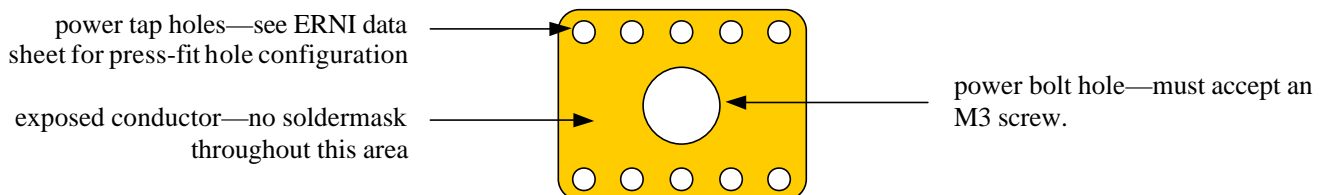
Recommended 12-layer stackup:

layer	layer name	layer type	net(s)	notes
1	surface	signal	TTC_R0-7, TTC_L0-7, misc	This layer faces the front of the subrack. Slot connectors and two LED's are placed on this layer.
2	ground	plane	GND	
3	power3	plane	VCC3	3.3V
4	power3	plane	VCC3	3.3V
5	ground	plane	GND	
6	signal6	signal	TCLK_P, TCLK_N	Only the TCLK pairs should be routed on layers 6 and 7
7	signal7	signal	TCLK_P, TCLK_N	
8	ground	plane	GND	
9	power5	plane	VCC5	5.0V
10	power5	plane	VCC5	5.0V
11	ground	plane	GND	
12	base	signal	TTC_R0-7, TTC_L0-7, misc	This layer faces the rear of the subrack. If possible, all components except slot connectors and two LED's should be placed on this layer.

VI. Decal (Part Footprint) Notes

See the **Footprint** and **Footprint Comment** columns in CRB_BOM_for_layout0.xls for decal details.

As shown in CRB_PowerAndMech_01.xls and below, the universal power site is designed to accommodate either a 10-pin ERNI power tap (ERNI# 114195) or an M3 screw. All holes are plated through holes. Conductor, in the arrangement shown below, must be exposed on both sides of the board. On inner plane layers not connected to the part, ample standard circular clearances around each hole are preferred. Please call if your CAD tools do not allow you to create the described footprint—an alternative may be acceptable.



***** **Thermal reliefs must not be used for any press-fit connections, including all holes of the universal power sites.** *****

If necessary, this requirement might be achieved by manual editing of Gerber files, e.g., by replacing thermal flashes for press-fit pins with circular flashes much smaller than the drill hole (e.g., 10 mil).

VII. Placement Notes

Reference designator bases can be used to identify parts that (typically) are placed near each other.

Notes for specific parts:

Type of Part, or Reference Designator	Notes
T13MP1	Place this monopin (test point) where it is readily accessible, e.g., in the unused slot 4 area.
PWD1-PWD4	Place one LED for each power supply on the surface and one LED for each power supply on the base. E.g., place the LED's in the unused slot 4 area.
T_CDC_POS	Each slot gets four capacitors, two per voltage (VCC and VCC3). For each voltage, place one capacitor at the top of the slot and one at the bottom of the slot. Do not share vias. Place vias as close as possible to capacitor pads, ideally on the same side of the capacitor.
PWCDC1-PWCDC18	Place one capacitor near each VCC5 and VCC3 universal power site.
TMRP1, TMRP2	Place terminator TermL and associated components at end of transmission lines (near slot 5). Place terminator TermR and associated components at end of transmission lines (near slot 21).
TMCDC1, TMCDC2	These CDC's for TermL and TermR should be located as close as possible to their connections on the resistor packs.
PWP1- PWP36	Place these universal power sites as shown in CRB_PowerAndMech_01.xls.
T_CRB_MOUNTING_HOLE: PWH2-PWH37	36 mounting holes are included in the netlist. The mounting hole size, plating, and arrangement should match that of the LHC standard VME64x backplane. Mounting holes for even slots are grounded. Those for odd slots are not connected. Reference designators may be omitted. Grounded holes should be labeled on the rear side of the board with "GND".

VIII. Routing Notes

Consult with the PCB manufacturer (Sanmina-SCI preferred) to obtain trace geometries for:

TCLK_P/TCLK_N	50 ohm single-ended (option 1)
TCLK_P/TCLK_N	100 ohm edge-coupled differential pairs (option 2)
TTC_R, TTC_L	100 ohm single-ended

TCLK Option 1 (this option seems more practical than option 2):

TCLK_P and TCLK_N nets (16 pairs total) are 100 ohm differential pairs but each pair is routed as two non-coupled 50 ohm single-ended lines. The lines should be routed with a trace width not used by any other signals, e.g., 6 mil. Center-to-center spacing should be sufficient that the two lines are not coupled, e.g., 75 mils. The PCB manufacturer should be told to size these traces for 50 ohm single-ended impedance. If possible, the 16 TCLK pairs should all have the same length, e.g., to within about 1 inch. Within-pair matching of trace length should be as close as possible, e.g., within 75 mils. A ground via should be added when changing layers, e.g., from horizontal to vertical routing.

TCLK Option 1 (requires removal of most connector pads on inner signal layers):

TCLK_P and TCLK_N nets (16 pairs total) are edge-coupled differential pairs and should be routed as such. They should be routed with a trace width not used by any other signals, e.g., 6 mil. Center-to-center spacing should be 14 mils or per PCB manufacturer recommendation. The PCB manufacturer should be told to size these traces for 100 ohm differential impedance. If possible, the 16 TCLK pairs should all have the same length, e.g., to within about 1 inch. Within-pair matching of trace length should be as close as possible, e.g., within 75 mils. A ground via should be added when changing layers, e.g., from horizontal to vertical routing.

TTC_R and TTC_L nets (16 nets total) are single-ended transmission lines. They should be routed with 7 mil traces or per PCB manufacturer recommendation. The PCB manufacturer should be told to size these traces for 100 ohm single-ended impedance. All of TTC_R0-7 and TTC_L0-7 must be routed on the same layer, either 1 or 12 (layer 1 is preferred). The lengths of the 16 TTC nets should be matched to within about one inch (which should happen naturally).

Connections to LED's should be at least one inch long to allow for soldering without excessive thermal stress.

BUSY_N nets are non-critical.

IX. Silkscreen Notes

Label all headers on silkscreen with:

- symbolic name
- pin 1
- GND pin or row (if any)
- VCC3 pin (if any)
- VCC5 pin (if any)

Label each slot with its slot number on both sides of the board.

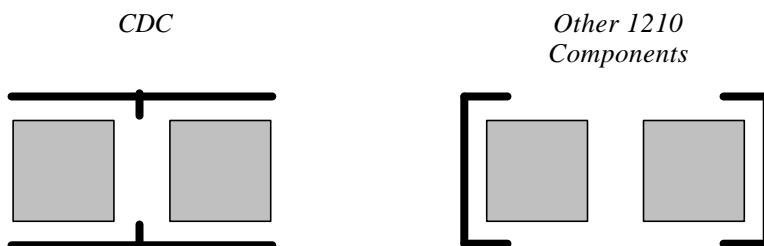
Label TIM and at least two ROD connectors on both sides of the board with:

- row letters, e.g., d c b a z
- min and max column numbers, e.g., 1 and 32

Label LED's with their corresponding supply voltage and net names:

- 5V (VCC5)
- 3.3V (VCC3)

Reference designators for CDC's may be omitted as long as the CDC decal (layout footprint) is distinguishable from those of other 1210 components (if any). E.g.,:



X. Contact Information

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