Notes for the CRB Preliminary Design Review

General

The CRB (CSC ROD Backplane) is a passive backplane that mounts in the J5/J6 area of a 9U VME64x subrack.

The major functions of the CRB are:

1. provide supplemental power distribution (+5V and +3.3V) to the ROD slots
2. distribute TTC signals from the TIM slot to the ROD slots
3. connect BUSY_N signals from ROD slots to the TIM slot

Recommended Documents at http://positron.ps.uci.edu/~pier/csc/sup/Support.html:

Document	Comment
Layout Notes	Describes CRB subsystems, symbolic netlist format, and PCB layout.
Power and Mechanical Overview	Presents the CRB mechanical arrangement and electrical calculations.
Symbolic Netlist	Provides electrical connection details.
System Power Estimate	Calculates expected supply currents.
Bus Bar Calculations	Calculates bus bar resistance, power dissipation, etc.

Major Design Considerations

Design Consideration	Comment
Is the TIM slot properly connected?	Click on the TimSlot13 link in Symbolic Netlist.
Are the ROD slots properly connected?	UCI will double check this, including on photoplots.
Has signal integrity been addressed?	See termination and loading notes below. See Layout Notes for trace impedances and PCB layer stackup.
Are there enough connector pins to carry the expected supply current?	See Power and Mechanical Overview. Expected current is about ½ the max allowed by the connectors. The resistance of the power plates and bus bars must be low enough that current does not flow disproportionately through a small subset of connector pins.
Are bus bars large enough.	See Power and Mechanical Overview and Bus Bar Calculations. See bus bar notes below.

Termination and Loading Notes

Signal	Type	Level	Board	Stub Length	Receiver or Driver	Termination
TCLK	pt-to-pt	5V PECL	ROD:	~1.5 inch	SN65LVDS34 receiver	100 ohm differential
			TM:	~1.5 inch	SN65LVDS34 receiver	none installed
TTC[7:0]	bussed	TTL	ROD:	~ 4 inch	XC2S150-5PQ208C FPGA	on backplane only
			TM:	~ 1.5 inch	SN74ABTE16245 transceiver	on backplane only
BUSY_N	pt-to-pt	TTL	ROD:	n/a	XC2S150-6FG256C FPGA	none
			TIM:	n/a	74LVT16244B receiver with 10k pullup to 3.3V	

Stub lengths include the signal length within the connector.

All receivers and drivers are 5V-tolerant regardless of supply voltage.

SN65LVDS34 receivers have a common-mode input range of –4V to +5V.

The TM will de-jitter TCLK using a VCXO-based PLL. The resulting clock will be used for Gb/s serializers/deserializers.

Backplane termination of TTC[7:0] is in the form of a SIP resistor pack with 160 ohms to +5V and 240 ohms to ground.

Bus Bar Notes:

"Measured" resistance values were measured with an HP3458A multimeter in four-wire mode.

VME and CRB power planes are assumed to be at nearly the same potential, because:

1. Copper power plates adjacent and parallel to slot 1-3 connect power supply voltages to both the VME and CRB backplanes.
2. bus-bar-to-power-plane resistance ("per slot") is less than one-tenth of slot-to-power-plane resistance
3. the resistance of bolted connections could not be measured, indicating that it is < ~.01 mohm

Due to mechanical constraints, the largest practical bus bar size is .35 x .35 inch. Calculations assume .3 x .3 inch bus bars.

The worst-case bus bar power dissipation (in the 5V bus bar) should be less than 1W.

The worst-case bus bar voltage drop should be less than 10 mV.

Bus bar power dissipation is concentrated near the lower-numbered slots, which are near the air-cooled power plates.

Power and Mechanical Overview compares VME backplane power and ground system measured resistances vs. calculated bus bar resistance.